Algorithms And Hardware Implementation Of Real Time

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VLSI and Hardware Implementations using Modern Machine Learning Methods IET
The theoretical basis of membrane computing was established in the early 2000s with fundamental research into the computational power, complexity aspects and relationships with other (un)conventional computing paradigms. Although this core theoretical research has continued to grow rapidly and vigorously, another area of investigation has since been added, focusing on the applications of this model in many areas, most prominently in systems and synthetic biology, engineering optimization, power system fault diagnosis and mobile robot controller design. The further development of these applications and their broad adoption by other researchers, as well as the expansion of the membrane computing modelling paradigm to other applications, call for a set of robust, efficient, reliable and easy-to-use tools supporting the most significant membrane computing models. This work provides comprehensive descriptions of such tools, making it a valuable resource for anyone interested in membrane computing models.
Thinking Machines McGraw Hill Professional
Machine learning is a potential solution to resolve bottleneck issues in VLSI via optimizing tasks in the design process. This book aims to provide the latest machine-learning–based methods, algorithms, architectures, and frameworks designed for VLSI design. The focus is on digital, analog, and mixed-signal design techniques, device modeling, physical design, hardware implementation, testability, reconfigurable design, synthesis and verification, and related areas. Chapters include case studies as well as novel research ideas in the given field. Overall, the book provides practical implementations of VLSI design, IC design, and hardware realization using machine learning techniques.
Features: Provides the details of state-of-the-art machine learning methods used in VLSI design Discusses hardware implementation and device modeling pertaining to machine learning algorithms Explores machine learning for various VLSI architectures and reconfigurable computing Illustrates the latest techniques for device size and feature optimization Highlights the latest case studies and reviews of the methods used for hardware implementation This book is aimed at researchers, professionals, and graduate students in VLSI, machine learning, electrical and electronic engineering, computer engineering, and hardware systems.
Learning in Energy-Efficient Neuromorphic Computing: Algorithm and Architecture Co-Design Computer ArithmeticAlgorithms and Hardware Implementations
Computer ArithmeticAlgorithms and Hardware ImplementationsSpringer Science & Business Media
Algorithms and Hardware Implementations Springer Nature
This text explains the fundamental principles of algorithms available for performing arithmetic operations on digital computers. These include basic arithmetic operations like addition, subtraction, multiplication, and division in fixed-point and floating-point number systems as well as more complex operations such as square root extraction and evaluation of exponential, logarithmic, and trigonometric functions. The algorithms described are independent of the particular technology employed for their implementation.
A Hardware Implementation of VHASH, a Universal Hashing Algorithm Using System Verilog Academic Press
An excellent introductory text, this book covers the basic theoretical, algorithmic and real-time aspects of digital signal processing (DSP). Detailed information is provided on off-line, real-time and DSP programming and the reader is effortlessly guided through advanced topics such as DSP hardware design, FIR and IIR filter design and difference equation manipulation.
Hardware Implementation of Cordic Algorithm in VHDL Springer Science & Business Media
Intelligent systems are now being used more commonly than in the past. These involve cognitive, evolving and artificial-life, robotic, and decision making systems, to name a few. Due to the tremendous speed of development, on both fundamental and technological levels, it is virtually impossible to offer an up-to-date, yet comprehensive overview of this field. Nevertheless, the need for a volume presenting recent developments and trends in this domain is huge, and the demand for such a volume is continually increasing in industrial and academic engineering 1 communities. Although there are a few volumes devoted to similar issues , none offer a comprehensive coverage of the field; moreover they risk rapidly becoming obsolete. The editors of this volume cannot pretend to fill such a large gap. However, it is the editors' intention to fill a significant part of this gap. A comprehensive coverage of the field should include topics such as neural networks, fuzzy systems, neuro-fuzzy systems, genetic algorithms, evolvable hardware, cellular automata-based systems, and various types of artificial life-system implementations, including autonomous robots. In this volume, we have focused on the first five topics listed above. The volume is composed of four parts, each part being divided into chapters, with the exception of part 4. In Part 1, the topics of "Evolvable Hardware and GAs" are addressed. In Chapter 1, "Automated Design Synthesis and Partitioning for Adaptive Reconfigurable Hardware", Ranga Vemuri and co-authors present state-of-the-art adaptive architectures, their classification, and their applications.
Studies on High-speed Hardware Implementation of Cryptographic Algorithms National Library of Canada = Bibliothèque nationale du Canada
Implement Finite-Field Arithmetic in Specific Hardware (FPGA and ASIC) Master cutting-edge electronic circuit synthesis and design with help from this detailed guide. Hardware Implementation of Finite-Field Arithmetic describes algorithms and circuits for executing finite-field operations, including addition, subtraction, multiplication, squaring, exponentiation, and division. This comprehensive resource begins with an overview of mathematics, covering algebra, number theory, finite fields, and cryptography. The book then presents algorithms which can be executed and verified with actual input data. Logic schemes and VHDL models are described in such a way that the corresponding circuits can be easily simulated and synthesized. The book concludes with a real-world example of a finite-field application--elliptic-curve cryptography. This is an essential guide for hardware engineers involved in the development of embedded systems. Get detailed coverage of: Modulo m reduction Modulo m addition, subtraction, multiplication, and exponentiation Operations over GF(p) and GF(pm) Operations over the commutative ring Zp[x]/f(x) Operations over the binary field GF(2m) using normal, polynomial, dual, and triangular
Hardware Implementation of Rijndael Encryption Algorithm CRC Press
This dissertation deals with the design of high-speed, bilinear algorithms for digital signal processing applications that are especially suited for implementation on dedicated hardware platforms. Bilinear algorithms exhibit a high degree of concurrency as all multiplication operations involved are independent of each other and can be computed at the same time. Consequently, the critical path delay for hardware implementations of these algorithms is very low. The algorithms developed here have other important properties such as a well defined recursive structure, modularity and low complexity. The first two properties are important for efficient mapping of the algorithm onto hardware and the last property helps in reducing hardware cost. Bilinear algorithms also have the advantage that two or more smaller algorithms can be used to obtain a larger, composite algorithm.
Machine Learning and Its Hardware Implementation Physica
Hacking and Phishing are major threats in today's informational world. Information security is a major concern for Information Technology (IT) specialists. Hackers and other untrusted parties try to access the confidential information using different hacking schemes. The only stable and long-term solution to security

threats is enforcing a strong and complex method of identity assurance. To achieve this, IT specialists incorporate different encryption techniques. In general, encryption refers to transforming the information into ciphered text using ciphers (algorithms). The ciphered text is readable, and only authenticated parties can decipher it. Hence, encryption is one of the major security solutions. Encryption involves a number of algorithms, one of which is cryptographic hashing. To enhance the performance of software algorithms, the developers rely on hardware accelerators. A hardware accelerator is a specific hardware unit apart from the CPU that performs a dedicated software or algorithmic implementation. In this project, a hardware implementation of a hashing algorithm known as VHASH is proposed. It was designed for exceptional performance on the systems that support 64-bit multiplication efficiently [5]. The hardware implementation of the VHASH algorithm involved modeling the algorithm in System Verilog hardware description language, validating and synthesizing it using a current hardware cell library. The testbench developed for verifying the design used System Verilog Functional Coverage to make sure the design was thoroughly verified. Verification was performed on Synopsys VCS® tool. The expected results used in validating the implementation were generated based on an existing python code for VMAC from [3]. The final phase of the project involved synthesizing the System Verilog model of VHASH algorithm towards LSI_10k technology library.

Hardware Implementation of Message Authentication Algorithms for Internet Security CRC Press

The security of sensitive information against 'prying eyes' has been of prime concern throughout the centuries. Therefore, a mechanism is required to guarantee the security and privacy of information. Under the existing circumstances cryptography is the only convenient method for protecting information transmitted through communication networks. The hardware implementation of cryptographic algorithms plays an important role because of growing requirements of high speed and high level secure communications. Accordingly, in this research attempt is taken to develop a faster and reliable cryptographic hardware by implementing one of the stream ciphers, RC4A in hardware. Verilog Hardware Description Language (HDL) and top down design methodology has been used to design the hardware implemented in this thesis. For hardware implementation of the design, an Altera Field Programmable Gate Array (FPGA) device, EP20K200EFC484-2X from APEX family, APEX 20KE, has been used. The designed hardware consumed 480 logic elements, 146 I/Os, and 10,240 bits memory. The hardware implementation achieved the data transfer rate of 22.28 MB/S in a clock frequency of 33.33 MHz. The implementation is able to support variable key lengths from 8 bits up to 512 bits. Unlike other stream ciphers, the proposed implementation generates two output streams at a time, whereas others generate only one output stream. So, user may use any of keystream which increase the unpredictability of the key as well as security.

A New Number Representation for Hardware Implementation of DSP Algorithms Springer Science & Business Media

Data transfer is becoming more and more essential these days with applications ranging from everyday social networking to important banking transactions. The data that is being sent or received shouldn't be in its original form but must be coded to avoid the risk of eavesdropping. A number of algorithms to encrypt and decrypt the data are available depending on the level of security to be achieved. Many of these algorithms require special hardware which makes them expensive for applications which require a low to medium level of data security. FPGAs are a cost effective way to implement such algorithms. We briefly survey several encryption/decryption algorithms and then focus on one of these, the Triple DES. This algorithm is currently used in the electronic payment industry as well as in applications such as Microsoft OneNote, Microsoft Outlook and Microsoft system center configuration manager to password protect user content and data. We implement the algorithm in a hardware description language, specifically VHDL and deploy it on an Altera DE1 board which uses a NIOS II soft core processor. The algorithm takes input encoded using a software based Huffman encoding to reduce its redundancy and compress the data. We analyze the results obtained from the implementation and discuss some methods to minimize attacks on the algorithm. Our VHDL implementation can also be ported to other hardware platforms.

An Efficient VHDL Description and Hardware Implementation of the Triple DES Algorithm John Wiley & Sons

Thinking Machines: Machine Learning and Its Hardware Implementation covers the theory and application of machine learning, neuromorphic computing and neural networks. This is the first book that focuses on machine learning accelerators and hardware development for machine learning. It presents not only a summary of the latest trends and examples of machine learning hardware and basic knowledge of machine learning in general, but also the main issues involved in its implementation. Readers will learn what is required for the design of machine learning hardware for neuromorphic computing and/or neural networks. This is a recommended book for those who have basic knowledge of machine learning or those who want to learn more about the current trends of machine learning. Presents a clear understanding of various available machine learning hardware accelerator solutions that can be applied to selected machine learning algorithms Offers key insights into the development of hardware, from algorithms, software, logic circuits, to hardware accelerators Introduces the baseline characteristics of deep neural network models that should be treated by hardware as well Presents readers with a thorough review of past research and products, explaining how to design through ASIC and FPGA approaches for target machine learning models Surveys current trends and models in neuromorphic computing and neural network hardware architectures Outlines the strategy for advanced hardware development through the example of deep learning accelerators

A Thesis

Digital video is becoming extremely important nowadays and its importance has greatly increased in the last two decades. Due to the rapid development of information and communication technologies, the demand for Ultra-High Definition (UHD) video applications is becoming stronger. However, the most prevalent video compression standard H.264/AVC released in 2003 is inefficient when it comes to UHD videos. The increasing desire for superior compression efficiency to H.264/AVC leads to the standardization of High Efficiency Video Coding (HEVC). Compared with the H.264/AVC standard, HEVC offers a double compression ratio at the same level of video quality or substantial improvement of video quality at the same video bitrate. Yet, HEVC/H.265 possesses superior compression efficiency, its complexity is several times more than H.264/AVC, impeding its high throughput implementation. Currently, most of the researchers have focused merely on algorithm level adaptations of HEVC/H.265 standard to reduce computational intensity without considering the hardware feasibility. What's more, the exploration of efficient hardware architecture design is not exhaustive. Only a few research works have been conducted to explore efficient hardware architectures of HEVC/H.265 standard. In this dissertation, we investigate efficient algorithm adaptations and hardware architecture design of HEVC intra encoders. We also explore the deep learning approach in mode prediction. From the algorithm point of view, we propose three efficient hardware-oriented algorithm adaptations, including mode reduction, fast coding unit (CU) cost estimation, and group-based CABAC (context-adaptive binary arithmetic coding) rate estimation. Mode reduction aims to reduce mode candidates of each prediction unit (PU) in the rate-distortion optimization (RDO) process, which is both computation-intensive and time-consuming. Fast CU cost estimation is applied to reduce the complexity in rate-distortion (RD) calculation of each CU. Group-based CABAC rate estimation is proposed to parallelize syntax elements processing to greatly improve rate estimation throughput. From the hardware design perspective, a fully parallel hardware architecture of HEVC intra encoder is developed to sustain UHD video compression at 4K@30fps. The fully parallel architecture introduces four prediction engines (PE) and each PE performs the full cycle of mode prediction, transform, quantization, inverse quantization, inverse transform, reconstruction, rate-distortion estimation independently. PU blocks with different PU sizes will be processed by the different prediction engines (PE) simultaneously. Also, an efficient hardware implementation of a group-based CABAC rate estimator is incorporated into the proposed HEVC intra encoder for accurate and high-throughput rate estimation. To take advantage of the deep learning approach, we also propose a fully connected layer based neural network (FCLNN) mode preselection scheme to reduce the number of RDO modes of luma prediction blocks. All angular prediction modes are classified into 7 prediction groups. Each group contains 3-5 prediction modes that exhibit a similar prediction angle. A rough angle detection algorithm is designed to determine the prediction direction of the current block, then a small scale FCLNN is exploited to refine the mode prediction.

Analysis and Hardware Implementation of Color Map Inversion Algorithms

The subject of this book is the analysis and design of digital devices that implement computer arithmetic. The book's presentation of high-level detail, descriptions, formalisms and design principles means that it can support many research activities in this field, with an emphasis on bridging the gap between algorithm optimization and hardware implementation. The author provides a unified view linking the domains of digital design and arithmetic algorithms, based on original formalisms and hardware description languages. A feature of the book is the large number of examples and the implementation details provided. While the author does not avoid high-level details, providing for example gate-level designs for all matrix/combinational arithmetic structures. The book is suitable for researchers and students engaged with hardware design in computer science and engineering. A feature of the book is the large number of examples and the implementation details provided. While the author does not avoid high-level details, providing for example gate-level designs for all matrix/combinational arithmetic structures. The book is suitable for researchers and students engaged with hardware design in computer science and engineering.

Algorithms and Hardware Co-design of HEVC Intra Encoders

Explains current co-design and co-optimization methodologies for building hardware neural networks and algorithms for machine learning applications This book focuses on how to build energy-efficient hardware for neural networks with learning capabilities—and provides co-design and co-optimization methodologies for building hardware neural networks that can learn. Presenting a complete picture from high-level algorithm to low-level implementation details, Learning in Energy-Efficient Neuromorphic Computing: Algorithm and Architecture Co-Design also covers many fundamentals and essentials in neural networks (e.g., deep learning), as well as hardware implementation of neural networks. The book begins with an overview of neural networks. It then discusses algorithms for utilizing and training rate-based artificial neural networks. Next comes an introduction to various options for executing neural networks, ranging from general-purpose processors to specialized hardware, from digital accelerator to analog accelerator. A design example on building energy-efficient accelerator for adaptive dynamic programming with neural networks is also presented. An examination of fundamental concepts and popular learning algorithms for spiking neural networks follows that, along with a look at the hardware for spiking neural networks. Then comes a chapter offering readers three design examples (two of which are based on conventional CMOS, and one on emerging nanotechnology) to implement the learning algorithm found in the previous chapter. The book concludes with an outlook on the future of neural network hardware. Includes cross-layer survey of hardware accelerators for neuromorphic algorithms Covers the co-design of architecture and algorithms with emerging devices for much-improved computing efficiency Focuses on the co-design of algorithms and hardware, which is especially critical for using emerging devices, such as traditional memristors or diffusive memristors, for neuromorphic computing Learning in Energy-Efficient Neuromorphic Computing: Algorithm and Architecture Co-Design is an ideal resource for researchers, scientists, software engineers, and hardware engineers dealing with the ever-increasing requirement on power consumption and response time. It is also excellent for teaching and training undergraduate and graduate students about the latest generation neural networks with powerful learning capabilities.

A Hardware Implementation of Blind Source Separation Algorithms

Software-based cryptography can be used for security applications where data traffic is not too large and low encryption rate is tolerable. But hardware methods are more suitable where speed and real-time encryption are needed. Until now, there has been no book explaining how cryptographic algorithms can be implemented on reconfigurable hardware devices. This book covers computational methods, computer arithmetic algorithms, and design improvement techniques needed to implement efficient cryptographic algorithms in FPGA reconfigurable hardware platforms. The author emphasizes the practical aspects of reconfigurable hardware design, explaining the basic mathematics involved, and giving a comprehensive description of state-of-the-art implementation techniques.

Theory, Algorithms and Hardware Design

The main objective of this thesis is the comprehensive analysis and synthesis with the hardwired square-rooting, believed to be the first subject to be implemented among various functions which are being evaluated mostly in software at present. Two new efficient algorithms for hardwired square-rooting, here called the algorithm G and algorithm T, have been developed and presented in the most detail. These use multiplication and no division. Furthermore, algorithm G possesses the property of quadratic convergence, a very important one for the machine of large word length as far as speed is concerned. Algorithm T is suitable for the machine of medium word length. (Author Modified Abstract).

Hardware Implementation of Intelligent Systems

"Three algorithms for computing the inverse of the forward printer map are studied in this thesis project. These are the Shepard's, Moving Matrix, and Iteratively Clustered Interpolation (ICI) algorithms. The algorithms are implemented in C and simulated in order to benchmark their relative accuracy, speed, and complexity."--Abstract.

Aspects of Fast Fourier Algorithms and Hardware Implementation of an Indexing Unit

Tiivistelmä: Tutkimuksia kryptografisten algoritmien laskennan nopeuttamisesta.

FPGA-based Hardware Implementation of Image Processing Algorithms for Real-time Vehicle Detection Applications

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