Power Integrity Modeling And Design For Semiconductors And Systems

2016 IEEE 20th Workshop on Signal and Power Integrity (SPI).
Principles of Power Integrity for PDN Design -- Simplified
Spectral, Convolution and Numerical Techniques in Circuit Theory
Power Integrity Modeling and Design for Semiconductors and Systems
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Power Integrity for I/O Interfaces
Integrity Issues & Simulation of Microelectronic Power Distribution Network
Digital Signal Integrity
Power Integrity Analysis and Management for Integrated Circuits (paperback)
Power Integrity for Nanoscale Integrated Systems
Power Distribution Network Design Methodologies
Power Integrity for I/O Interfaces
System Level Power Integrity Transient Analysis Using a Physics-based Approach
Tensorial Analysis of Networks (TAN) Modelling for PCB Signal Integrity and EMC Analysis
Semiconductor Modeling:
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High Speed Digital Design
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Signal Integrity Effects in Custom IC and ASIC Designs
Integrated Circuit and System Design: Power and Timing Modeling, Optimization and Simulation
Modeling and Design of Electromagnetic Compatibility for High-Speed Printed Circuit Boards and Packaging
Silicon Germanium
Electrical Modeling and Signal/power Integrity Design in Three-dimensional Memory Packaging
Electrical Modeling and Design for 3D System Integration
High-Speed Signaling
Datenintensive Anwendungen designen
Electrical Design of Through Silicon Via
2018 IEEE 22nd Workshop on Signal and Power Integrity (SPI)
2017 IEEE 21st Workshop on Signal and Power Integrity (SPI)
High-Speed Signaling
2020 IEEE 24th Workshop on Signal and Power Integrity (SPI)
Modeling and Design Techniques for Improved Delay, Power and Signal Integrity in Nanoscale VLSI.
2022 IEEE 26th Workshop on Signal and Power Integrity (SPI)
PCB Design for Real-World EMI Control
Outlines and Highlights for Power Integrity Modeling and Design for Semiconductors and Systems by Engin, Isbn
Electrical Modeling and Design for 3D System Integration
Design and Modeling for 3D ICs and Interposers
2021 IEEE 25th Workshop on Signal and Power Integrity (SPI)

SAWYER PITTS

2016 IEEE 20th Workshop on Signal and Power Integrity (SPI). O'Reilly
Characterization, modeling and design for signal and power integrity of electronic systems Modeling, simulation and measurement of electrical interconnect performance at chip, board and package levels Innovative CAD concepts and algorithms Applications to computing devices, mobile devices, automotive aerospace Optical interconnection technology on component and board level
Principles of Power Integrity for PDN Design -- Simplified Springer
Characterization, modeling and design for signal and power integrity of electronic systems Modeling, simulation and measurement of electrical interconnect performance at chip, board and package levels Innovative CAD concepts and algorithms Applications to computing devices, mobile devices, automotive aerospace.
Spectral, Convolution and Numerical Techniques in Circuit Theory Pearson
"With decreasing supply voltage level and massive demanding current on system chipset, power integrity design becomes more and more critical for system stability. The ultimate goal of well-designed power delivery network (PDN) is to deliver desired voltage level from the source to destination, in other words, to minimize voltage noise delivered to digital devices. The thesis is composed of three parts. The first part focuses on-die level power models including simplified chip power model (CPM) for system level analysis and the worst scenario current profile. The second part of this work introduces the physics-based equivalent circuit model to simplify the passive PDN model to RLC circuit netlist, to be compatible with any spice simulators and tremendously boost simulation speed. Then a novel system/chip level end-to-end transient model is proposed, including the die model and passive PDN model discussed in previous two chapters as well as a SIMPLIS based small signal VRM model. In the last part of the thesis, how to model voltage regulator module (VRM) is explicitly discussed. Different linear approximated VRM modeling approaches have been compared with the SIMPLIS small signal VRM model in both frequency domain and time domain. The comparison provides PI engineers a guideline to choose specific VRM model under specific circumstances. Finally yet importantly, a PDN optimization example was given. Other than previous PDN optimization approaches, a novel hybrid target impedance concept was proposed in this thesis, in order to improve system level PDN optimization process"--Abstract, page iv.
Power Integrity Modeling and Design for Semiconductors and Systems McGraw Hill Professional
Characterization, modeling and design for signal and power integrity of electronic systems Modeling, simulation and measurement of electrical interconnect performance at chip, board and package levels Innovative CAD concepts and algorithms Applications to computing devices, mobile devices, automotive aerospace
Power Integrity Modeling and Design for Semiconductors and Systems John Wiley & Sons
Foreword by Joungho Kim The Hands-On Guide to Power Integrity in Advanced Applications, from Three Industry Experts In this book, three industry experts introduce state-of-the-art power integrity design techniques for today's most advanced digital systems, with real-life, system-level examples. They introduce a powerful approach to unifying power and signal integrity design that can identify signal impediments earlier, reducing cost and improving reliability. After introducing high-speed, single-ended and differential I/O interfaces, the authors describe on-chip, package, and PCB power distribution networks (PDNs) and signal networks, carefully reviewing their interactions. Next, they walk through end-to-end PDN and signal network design in frequency domain, addressing crucial parameters such as self and transfer impedance. They thoroughly address modeling and characterization of on-chip components of PDNs and signal networks, evaluation of power-to-signal coupling coefficients, analysis of Simultaneous Switching Output (SSO) noise, and many other topics. Coverage includes • The exponentially growing challenge of I/O power integrity in high-speed digital systems • PDN noise analysis and its timing impact for single-ended and differential interfaces • Concurrent design and co-simulation techniques for evaluating all power integrity effects on signal integrity • Time domain gauges for designing and optimizing components and systems • Power/signal integrity interaction mechanisms, including power noise coupling onto signal trace and noise amplification through signal resonance • Performance impact due to Inter Symbol Interference (ISI), crosstalk, and SSO noise, as well as their interactions • Validation techniques, including low impedance VNA measurements, power noise measurements, and characterization of power-to-signal coupling effects Power Integrity for I/O Interfaces will be an indispensable resource for everyone concerned with power integrity in cutting-edge digital designs, including system design and hardware engineers, signal and power integrity engineers, graduate students, and researchers.
Power Integrity for I/O Interfaces World Scientific
3D Integration is being touted as the next semiconductor revolution. This book provides a comprehensive coverage on the design and modeling aspects of 3D integration, in particularly, focus on its electrical behavior. Looking from the perspective the Silicon Via (TSV) and Glass Via (TGV) technology, the book introduces 3DICs and Interposers as a technology, and presents its application in numerical modeling, signal integrity, power integrity and thermal integrity. The authors underscored the potential of this technology in design exchange formats and power distribution.
Integrity Issues & Simulation of Microelectronic Power Distribution Network Springer
Characterization, modeling and design for signal and power integrity of electronic systems Modeling, simulation and measurement of electrical interconnect performance at chip, board and package levels Innovative CAD concepts and algorithms Applications to computing devices, mobile devices, automotive aerospace Optical interconnection technology on component and board level
Digital Signal Integrity Pearson Education
This book constitutes the thoroughly refereed post-conference proceedings of 19th International Workshop on Power and Timing Modeling, Optimization and Simulation, PATMOS 2009, featuring Integrated Circuit and System Design, held in Delft, The Netherlands during September 9-11, 2009. The 26 revised full papers and 10 revised poster papers presented were carefully reviewed and selected from numerous submissions. The papers are organized in topical sections on variability & statistical timing, circuit level techniques, power management, low power circuits & technology, system level techniques, power & timing optimization techniques, self-timed circuits, low power circuit analysis & optimization, and low power design studies.
Power Integrity Analysis and Management for Integrated Circuits (paperback) Intl. Engineering Consortiu
The First Comprehensive, Example-Rich Guide to Power Integrity Modeling Professionals such as signal integrity engineers, package designers, and system architects need to thoroughly understand signal and power integrity issues in order to successfully design packages and boards for high speed systems. Now, for the first time, there's a complete guide to power integrity modeling: everything you need to know, from the basics through the state of the art. Using realistic case studies and downloadable software examples, two leading experts demonstrate today's best techniques for designing and modeling interconnects to efficiently distribute power and minimize noise. The authors carefully introduce the core concepts of power distribution design, systematically present and compare leading techniques for modeling noise, and link these techniques to specific applications. Their many examples range from the simplest (using analytical equations to compute power supply noise) through complex system-level applications. The authors Introduce power delivery network components, analysis, high-frequency measurement, and modeling requirements Thoroughly explain modeling of power/ground planes, including plane behavior, lumped modeling, distributed circuit-based approaches, and much more Offer in-depth coverage of simultaneous switching noise, including modeling for return currents using time- and frequency-domain analysis

Introduce several leading time-domain simulation methods, such as macromodeling, and discuss their advantages and disadvantages Present the application of the modeling methods on several advanced case studies that include high-speed servers, high-speed differential signaling, chip package analysis, materials characterization, embedded decoupling capacitors, and electromagnetic bandgap structures This book's system-level focus and practical examples will make it indispensable for every student and professional concerned with power integrity, including electrical engineers, system designers, signal integrity engineers, and materials scientists. It will also be valuable to developers building software that helps to analyze high-speed systems.

Power Integrity for Nanoscale Integrated Systems Power Integrity Modeling and Design for Semiconductors and Systems

Proper design of printed circuit boards can make the difference between a product passing emissions requirements during the first cycle or not. Traditional EMC design practices have been simply rule-based, that is, a list of rules-of-thumb are presented to the board designers to implement. When a particular rule-of-thumb is difficult to implement, it is often ignored. After the product is built, it will often fail emission requirements and various time consuming and costly add-ons are then required. Proper EMC design does not require advanced degrees from universities, nor does it require strenuous mathematics. It does require a basic understanding of the underlying principles of the potential causes of EMC emissions. With this basic understanding, circuit board designers can make trade-off decisions during the design phase to ensure optimum EMC design. Consideration of these potential sources will allow the design to pass the emissions requirements the first time in the test laboratory. A number of other books have been published on EMC. Most are general books on EMC and do not focus on printed circuit board is intended to help EMC engineers and design design. This book engineers understand the potential sources of emissions and how to reduce, control, or eliminate these sources. This book is intended to be a 'hands-on' book, that is, designers should be able to apply the concepts in this book directly to their designs in the real-world.

Power Distribution Network Design Methodologies John Wiley & Sons

High Speed Digital Design discusses the major factors to consider in designing a high speed digital system and how design concepts affect the functionality of the system as a whole. It will help you understand why signals act so differently on a high speed digital system, identify the various problems that may occur in the design, and research solutions to minimize their impact and address their root causes. The authors offer a strong foundation that will help you get high speed digital system designs right the first time. Taking a systems design approach, High Speed Digital Design offers a progression from fundamental to advanced concepts, starting with transmission line theory, covering core concepts as well as recent developments. It then covers the challenges of signal and power integrity, offers guidelines for channel modeling, and optimizing link circuits. Tying together concepts presented throughout the book, the authors present Intel processors and chipsets as real-world design examples. Provides knowledge and guidance in the design of high speed digital circuits Explores the latest developments in system design Covers everything that encompasses a successful printed circuit board (PCB) product Offers insight from Intel insiders about real-world high speed digital design

Power Integrity for I/O Interfaces Prentice Hall

State-of-the-art techniques for predicting and achieving target performance levels Theory, practice, general signal integrity issues, and leading-edge experimental techniques Model and simulate high-speed digital systems for maximum performance Maximizing the performance of digital systems means optimizing their high-speed interconnections. Digital Signal Integrity gives engineers all the theory and practical methods they need to accurately model and simulate those interconnections and predict real-world performance. Whether you're modeling microprocessors, memories, DSPs, or ASICs, these techniques will get you to market faster with greater reliability. Coverage includes: In-depth reviews of inductance, capacitance, resistance, single and multiconductor transmission lines, generalized termination schemes, crosstalk, differential signaling, and other modeling/simulation issues Multiconductor interconnects: packages, sockets, connectors and buses Modal decomposition: understanding the outputs generated by commercial modeling software Layer peeling with time-domain reflectometry: its power and limitations Experimental techniques for characterizing interconnect parasitics In Digital Signal Integrity, Motorola senior engineer Brian Young presents broad coverage of modeling from data obtained through electromagnetic simulation, transmission line theory, frequency and time-domain modeling, analog circuit simulation, digital signaling, and architecture. Young offers a strong mathematical foundation for every technique, as well as over 100 end-of-chapter problems. If you're stretching the performance envelope, you must be able to rely on your models and simulations. With this book, you can.

System Level Power Integrity Transient Analysis Using a Physics-based Approach Prentice Hall

The First Comprehensive, Example-Rich Guide to Power Integrity Modeling Professionals such as signal integrity engineers, package designers, and system architects need to thoroughly understand signal and power integrity issues in order to successfully design packages and boards for high speed systems. Now, for the first time, there's a complete guide to power integrity modeling: everything you need to know, from the basics through the state of the art. Using realistic case studies and downloadable software examples, two leading experts demonstrate today's best techniques for designing and modeling interconnects to efficiently distribute power and minimize noise. The authors carefully introduce the core concepts of power distribution design, systematically present and compare leading techniques for modeling noise, and link these techniques to specific applications. Their many examples range from the simplest (using analytical equations to compute power supply noise) through complex system-level applications. The authors Introduce power delivery network components, analysis, high-frequency measurement, and modeling requirements Thoroughly explain modeling of power/ground planes, including plane behavior, lumped modeling, distributed circuit-based approaches, and much more Offer in-depth coverage of simultaneous switching noise, including modeling for return currents using time- and frequency-domain analysis Introduce several leading time-domain simulation methods, such as macromodeling, and discuss their advantages and disadvantages Present the application of the modeling methods on several advanced case studies that include high-speed servers, high-speed differential signaling, chip package analysis, materials characterization, embedded decoupling capacitors, and electromagnetic bandgap structures This book's system-level focus and practical examples will make it indispensable for every student and professional concerned with power integrity, including electrical engineers, system designers, signal integrity engineers, and materials scientists. It will also be valuable to developers building software that helps to analyze high-speed systems.

Tensorial Analysis of Networks (TAN) Modelling for PCB Signal Integrity and EMC Analysis Springer

New System-Level Techniques for Optimizing Signal/Power Integrity in High-Speed Interfaces--from Pioneering Innovators at Rambus, Stanford, Berkeley, and MIT As data communication rates accelerate well into the multi-gigahertz range, ensuring signal integrity both on- and off-chip has become crucial. Signal integrity can no longer be addressed solely through improvements in package or board-level design: Diverse engineering teams must work together closely from the earliest design stages to identify the best system-level solutions. In High-Speed Signaling, several of the field's most respected practitioners and researchers introduce cutting-edge modeling, simulation, and optimization techniques for meeting this challenge. Edited by pioneering experts Drs. Dan Oh and Chuck Yuan, these contributors explain why noise and jitter are no longer separable, demonstrate how to model their increasingly complex interactions, and thoroughly introduce a new simulation methodology for predicting link-level performance with unprecedented accuracy. The authors address signal integrity from architecture through high-volume production, thoroughly discussing design, implementation, and verification. Coverage includes New advances in passive-channel modeling, power-supply noise and jitter modeling, and system margin prediction Methodologies for balancing system voltage and timing budgets to improve system robustness in high-volume manufacturing Practical, stable formulae for converting key network parameters Improved solutions for difficult problems in the broadband modeling of interconnects Equalization techniques for optimizing channel performance Important new insights into the relationships between jitter and clocking topologies New on-chip measurement techniques for in-situ link performance testing Trends and future directions in signal integrity engineering High-Speed Signaling thoroughly introduces new techniques pioneered at Rambus and other leading high-tech companies and universities: approaches that have never before been presented with this much practical detail. It will be invaluable to everyone concerned with signal integrity, including signal and power integrity engineers, high-speed I/O circuit designers, and system-level board design engineers.

Semiconductor Modeling: Springer Science & Business Media

Discusses process variation, model accuracy, design flow and many other practical engineering, reliability and manufacturing issues Gives a good overview for a person who is not an expert in modeling and simulation, enabling them to extract the necessary information to competently use modeling and simulation programs Written for engineering students and product design engineers

2017 IEEE 21st Workshop on Signal and Power Integrity (SPI) Pearson Education

Power Integrity Modeling and Design for Semiconductors and SystemsPearson Education

High Speed Digital Design John Wiley & Sons

Through Silicon Via (TSV) is a key technology for realizing three-dimensional integrated circuits (3D ICs) for future high-performance and low-power systems with small form factors. This book covers both qualitative and quantitative approaches to give insights of modeling TSV in a various viewpoints such as signal integrity, power integrity and thermal integrity. Most of the analysis in this book includes simulations, numerical modelings and measurements for verification. The author and co-authors in each chapter have studied deep into TSV for many years and the accumulated technical know-hows and tips for related subjects are comprehensively covered.

Power Integrity Analysis and Management for Integrated Circuits Springer Science & Business Media

Foreword by Joungho Kim The Hands-On Guide to Power Integrity in Advanced Applications, from Three Industry Experts In this book, three industry experts introduce state-of-the-art power integrity design techniques for today's most advanced digital systems, with real-life, system-level examples. They introduce a powerful approach to unifying power and signal integrity design that can identify signal impediments earlier, reducing cost and improving reliability. After introducing high-speed, single-ended and differential I/O interfaces, the authors describe on-chip, package, and PCB power distribution networks (PDNs) and signal networks, carefully reviewing their interactions. Next, they walk through end-to-end PDN and signal network design in frequency domain, addressing crucial parameters such as self and transfer impedance. They thoroughly address modeling and characterization of on-chip components of PDNs and signal networks, evaluation of power-to-signal coupling coefficients, analysis of Simultaneous Switching Output (SSO) noise, and many other topics. Coverage includes The exponentially growing challenge of I/O power integrity in high-speed digital systems PDN noise analysis and its timing impact for single-ended and differential interfaces Concurrent design and co-simulation techniques for evaluating all power integrity effects on signal integrity Time domain gauges for designing and optimizing components and systems Power/signal integrity interaction mechanisms, including power noise coupling onto signal trace and noise amplification through signal resonance Performance impact due to Inter Symbol Interference (ISI), crosstalk, and SSO noise, as well as their interactions Validation techniques, including low impedance VNA measurements, power noise measurements, and characterization of power-to-signal coupling effects Power Integrity for I/O Interfaces will be an indispensable resource for everyone concerned with power integrity in cutting-edge digital designs, including system design and hardware engineers, signal and power integrity engineers, graduate students, and researchers.

2016 IEEE 20th Workshop on Signal and Power Integrity (SPI) Academic Internet Pub Incorporated

Modeling and Design of Electromagnetic Compatibility for High-Speed Printed Circuit Boards and Packaging presents the electromagnetic modelling and design of three major electromagnetic compatibility (EMC) issues related to the high-speed printed circuit board (PCB) and electronic packages: signal integrity (SI), power integrity (PI), and electromagnetic interference (EMI). The emphasis is put on two essential passive components of PCBs and packages: the power distribution network and the signal distribution network. This book includes two parts. Part one talks about the field-circuit hybrid methods used for the EMC modeling, including the modal method, the integral equation method, the cylindrical wave expansion method and the de-embedding method. Part two illustrates EMC design methods and explores the applications of novel metamaterials and two-dimensional materials on traditional EMC problems. This book is designed to enhance worthwhile electromagnetic theory and mathematical methods for practical engineers and to train students with advanced EMC applications.

Signal Integrity Effects in Custom IC and ASIC Designs Elsevier

New advanced modeling methods for simulating the electromagnetic properties of complex three-dimensional electronic systems Based on the author's extensive research, this book sets forth tested and proven electromagnetic modeling and simulation methods for analyzing signal and power integrity as well as electromagnetic interference in large complex electronic interconnects, multilayered package structures, integrated circuits, and printed circuit boards. Readers will discover the state of the technology in electronic package integration and printed circuit board simulation and modeling. In addition to popular full-wave electromagnetic computational methods, the book presents new, more sophisticated modeling methods, offering readers the most advanced tools for analyzing and designing large complex electronic structures. Electrical Modeling and Design for 3D System Integration begins with a comprehensive review of current modeling and simulation methods for signal integrity, power integrity, and electromagnetic compatibility. Next, the book guides readers through: The macromodeling technique used in the electrical and electromagnetic modeling and simulation of complex interconnects in three-dimensional integrated systems The semi-analytical scattering matrix method based on the N-body scattering theory for modeling of three-dimensional electronic package and multilayered printed circuit boards with multiple vias Two- and three-dimensional integral equation methods for the analysis of power distribution networks in three-dimensional package integrations The physics-based algorithm for extracting the equivalent circuit of a complex power distribution network in three-dimensional integrated systems and printed circuit boards An equivalent circuit model of through-silicon vias Metal-oxide-semiconductor capacitance effects of through-silicon vias Engineers, researchers, and students can turn to this

book for the latest techniques and methods for the electrical modeling and design of electronic packaging, three-dimensional electronic integration, integrated circuits, and printed circuit boards.