Built In Test For Vlsi Pseudorandom Techniques

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IEEE VLSI Test Symposium
Sixth International Conferencew on Information Technology
Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits
Testfreundliche Synthese hochintegrierter Schaltungen
Test Resource Partitioning for System-on-a-Chip
SOC Design Methodologies
Proceedings of the Estonian Academy of Sciences, Engineering
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OSBORN TRUJILLO

VLSI Test Principles and Architectures ASM International
Managing the power consumption of circuits and systems is now considered one of the most important challenges for the semiconductor industry. Elaborate power management strategies, such as dynamic voltage scaling, clock gating or power gating techniques, are used today to control the power dissipation during functional operation. The usage of these strategies has various implications on manufacturing test, and power-aware test is therefore increasingly becoming a major consideration during design-for-test and test preparation for low power devices. This book explores existing solutions for power-aware test and design-for-test of conventional circuits and systems, and surveys test strategies and EDA solutions for testing low power devices.

An Introduction to Logic Circuit Testing CRC Press
Modern electronics testing has a legacy of more than 40 years. The introduction of new technologies, especially nanometer technologies with 90nm or smaller geometry, has allowed the semiconductor industry to keep pace with the increased performance-capacity demands from consumers. As a result, semiconductor test costs have been growing steadily and typically amount to 40% of today's overall product cost. This book is a comprehensive guide to new VLSI Testing and Design-for-Testability techniques that will allow students, researchers, DFT practitioners, and VLSI designers to master quickly System-on-Chip Test architectures, for test debug and diagnosis of digital, memory, and analog/mixed-signal designs. Emphasizes VLSI Test principles and Design for Testability architectures, with numerous illustrations/examples. Most up-to-date coverage available, including Fault Tolerance, Low-Power Testing, Defect and Error Tolerance, Network-on-Chip (NOC) Testing, Software-Based Self-Testing, FPGA Testing, MEMS Testing, and System-In-Package (SIP) Testing, which are not yet available in any testing book. Covers the entire spectrum of VLSI testing and DFT architectures, from digital and analog, to memory circuits, and fault diagnosis and self-repair from digital to memory circuits. Discusses future nanotechnology test trends and challenges facing the nanometer design era; promising nanotechnology test techniques, including Quantum-Dots, Cellular Automata, Carbon-Nanotubes, and Hybrid Semiconductor/Nanowire/ Molecular Computing. Practical problems at the end of each chapter for students.

Electronic Materials Handbook North Holland
A recent technological advance is the art of designing circuits to test themselves, referred to as a Built-In Self-Test. This book is written from a designer's perspective and describes the major BIST approaches that have been proposed and implemented, along with their advantages and limitations.

VLSI Testing Springer-Verlag

The 11 th IFIP International Conference on Very Large Scale Integration, in Montpellier, France, December 3-5,2001, was a great success. The main focus was about IP Cores, Circuits and System Designs & Applications as well as SOC Design Methods and CAD. This book contains the best papers (39 among 70) that have been presented during the conference. Those papers deal with all aspects of importance for the design of the current and future integrated systems. System on Chip (SOC) design is today a big challenge for designers, as a SOC may contain very different blocks, such as microcontrollers, DSPs, memories including embedded DRAM, analog, FPGA, RF front-ends for wireless communications and integrated sensors. The complete design of such chips, in very deep submicron technologies down to 0.13 mm, with several hundreds of millions of transistors, supplied at less than 1 Volt, is a very challenging task if design, verification, debug and industrial test are considered. The microelectronic revolution is fascinating; 55 years ago, in late 1947, the transistor was invented, and everybody knows that it was by William Shockley, John Bardeen and Walter H. Brattein, Bell Telephone Laboratories, which received the Nobel Prize in Physics in 1956. Probably, everybody thinks that it was recognized immediately as a major invention.

Testability Concepts for Digital ICs IET

A pragmatic approach to testing electronic systems As we move ahead in the electronic age, rapid changes in technology pose an ever-increasing number of challenges in testing electronic products. Many practicing engineers are involved in this arena, but few have a chance to study the field in a systematic way-learning takes place on the job. By covering the fundamental disciplines in detail, Principles of Testing Electronic Systems provides design engineers with the much-needed knowledge base. Divided into five major parts, this highly useful reference relates design and tests to the development of reliable electronic products; shows the main vehicles for design verification; examines designs that facilitate testing; and investigates how testing is applied to random logic, memories, FPGAs, and microprocessors. Finally, the last part offers coverage of advanced test solutions for today's very deep submicron designs. The authors take a phenomenological approach to the subject matter while providing readers with plenty of opportunities to explore the foundation in detail. Special features include: * An explanation of where a test belongs in the design flow * Detailed discussion of scan-path and ordering of scan-chains * BIST solutions for embedded logic and memory blocks * Test methodologies for FPGAs * A chapter on testing system on a chip * Numerous references

Optimal Design of VLSI Structures with Built-in Self Test Based on Reduced Pseudo-exhaustive Testing Springer

This book covers the spectrum of the testing problem. Areas covered include fault modeling, test generation, fault simulation, memory testing, design for testability, testability measures, PLA testing, and test equipment. The use of this volume will provide a good insight into the VLSI challenges in

the area of testing - an area that has become increasingly important due to the emphasis on quality of VLSI products, and the associated costs. As a result, there has been a rapid expansion in the technologies associated with testing, and it is this technological growth which is reflected in the contributions to this volume.

Principles of Testing Electronic Systems
Springer Science & Business Media
An Introduction to Logic Circuit Testing provides a detailed coverage of techniques for test generation and testable design of digital electronic circuits/systems. The material covered in the book should be sufficient for a course, or part of a course, in digital circuit testing for senior-level undergraduate and first-year graduate students in Electrical Engineering and Computer Science. The book will also be a valuable resource for engineers working in the industry. This book has four chapters. Chapter 1 deals with various types of faults that may occur in very large scale integration (VLSI)-based digital circuits. Chapter 2 introduces the major concepts of all test generation techniques such as redundancy, fault coverage, sensitization, and backtracking. Chapter 3 introduces the key concepts of testability, followed by some ad hoc design-for-testability rules that can be used to enhance testability of combinational circuits. Chapter 4 deals with test generation and response evaluation techniques used in BIST (built-in self-test) schemes for VLSI chips. Table of Contents: Introduction / Fault Detection in Logic Circuits / Design for Testability / Built-in Self-Test / References

System-on-Chip Test Architectures Springer
Test functions (fault detection, diagnosis, error correction, repair, etc.) that are applied concurrently while the system continues its intended function are defined as on-line testing. In its expanded scope, on-line testing includes the design of concurrent error checking subsystems that can be themselves self-checking, fail-safe systems that continue to function correctly even after an error occurs, reliability monitoring, and self-test and fault-tolerant designs. On-Line Testing for VLSI contains a selected set of articles that discuss many of the modern aspects of on-line testing as faced today. The contributions are largely derived from recent IEEE International On-Line Testing Workshops. Guest editors Michael Nicolaidis, Yervant Zorian and Dhiraj Pradhan organized the articles into six chapters. In the first chapter the editors introduce a large number of approaches with an expanded bibliography in which some references date back to the sixties. On-Line Testing for VLSI is an edited volume of original research comprising invited contributions by leading researchers.

Arithmetic Built-in Self-test for Embedded Systems Springer
The 7th International Conference on Information Technology (CIT 2004) was held in Hyderabad, India, during December 20–23, 2004. The CIT 2004 was a forum where researchers from various areas of information technology and its applications could stimulate and exchange ideas on technological advancements. CIT, organizedby the Orissa InformationTechnologySociety (OITS), has emerged as one of the major international conferences

in India and is fast becoming the premier forum for the presentation of the latest research and development in the critical area of information technology. The last six conferences attracted reputed researchers from around the world, and CIT 2004 took this trend forward. This conference focused on the latest research ?ndings on all topics in the area of information technology. Although the natural focus was on computer science issues, research results contributed from management, business and other disciplines formed an integral part. We received more than 200 papers from over 27 countries in the areas of com- tational intelligence, neural networks, mobile and adhoc networks, security, databases, softwareengineering,signal andimageprocessing,andInternetandWWW-basedc- puting. The programme committee, consisting of eminent researchers, academicians and practitioners, ?nally selected 43 full papers on the basis of reviewer grades. This proceedings contains the research papers selected for presentation at the c- ference and this is the ?rst time that the proceedingshave been published in the Lecture Notes in Computer Science (LNCS) series. The poster papers are being printed as a separate conference proceedings.

A Designer’s Guide to Built-In Self-Test Springer-Verlag

Test Resource Partitioning for System-on-a-Chip is about test resource partitioning and optimization techniques for plug-and-play system-on-a-chip (SOC) test automation. Plug-and-play refers to the paradigm in which core-to-core interfaces as well as core-to-SOC logic interfaces are standardized, such that cores can be easily plugged into "virtual sockets" on the SOC design, and core tests can be plugged into the SOC during test without substantial effort on the part of the system integrator. The goal of the book is to position test resource partitioning in the context of SOC test automation, as well as to generate interest and motivate research on this important topic. SOC integrated circuits composed of embedded cores are now commonplace. Nevertheless, There remain several roadblocks to rapid and efficient system integration. Test development is seen as a major bottleneck in SOC design, and test challenges are a major contributor to the widening gap between design capability and manufacturing capacity. Testing SOCs is especially challenging in the absence of standardized test structures, test automation tools, and test protocols. Test Resource Partitioning for System-on-a-Chip responds to a pressing need for a structured methodology for SOC test automation. It presents new techniques for the partitioning and optimization of the three major SOC test resources: test hardware, testing time and test data volume. Test Resource Partitioning for System-on-a-Chip paves the way for a powerful integrated framework to automate the test flow for a large number of cores in an SOC in a plug-and-play fashion. The framework presented allows the system integrator to reduce test cost and meet short time-to-market requirements.

VLSI Testing Elsevier

Volume 1: Packaging is an authoritative reference

source of practical information for the design or process engineer who must make informed day-to-day decisions about the materials and processes of microelectronic packaging. Its 117 articles offer the collective knowledge, wisdom, and judgement of 407 microelectronics packaging experts-authors, co-authors, and reviewers-representing 192 companies, universities, laboratories, and other organizations. This is the inaugural volume of ASMAs all-new ElectronicMaterials Handbook series, designed to be the Metals Handbook of electronics technology. In over 65 years of publishing the Metals Handbook, ASM has developed a unique editorial method of compiling large technical reference books. ASMAs access to leading materials technology experts enables to organize these books on an industry consensus basis. Behind every article. Is an author who is a top expert in its specific subject area. This multi-author approach ensures the best, most timely information throughout. Individually selected panels of 5 and 6 peers review each article for technical accuracy, generic point of view, and completeness.Volumes in the Electronic Materials Handbook series are multidisciplinary, to reflect industry practice applied in integrating multiple technology disciplines necessary to any program in advanced electronics. Volume 1: Packaging focusing on the middle level of the electronics technology size spectrum, offers the greatest practical value to the largest and broadest group of users. Future volumes in the series will address topics on larger (integrated electronic assemblies) and smaller (semiconductor materials and devices) size levels.

Advanced Simulation and Test Methodologies for VLSI Design Springer Science & Business Media

Eingebettete Systeme übernehmen zentrale Steueraufgaben im täglichen Leben. In der Energieversorgung oder im Transportwesen würde ein Ausfall der Systeme fatale Auswirkungen haben. Der Nutzer verlässt sich aber auf ein fehlerfreies Funktionieren des Systems. Die Funktionstüchtigkeit der Schaltkreise zu garantieren, ist das Ziel des Testens – und das mit geringen Kosten, da jeder Chip nach der Produktion separat getestet werden muss.

Introduction to VLSI Testing Springer Science & Business Media

A distinctive feature of modern computer equipment development is the continuous increase in functionality and complexity of computer components. As a result of these advances, very large-scale integration (VLSI) circuits have found extensive application in the manufacture of computer products, personal computers included. Among a variety of recently evolved VLSI design technologies, the self-test VLSI design has gained particular prominence. design. A summary is given on self-test VLSI design results that have been obtained by scientists in leading scientific centres for computer integrated circuits. Emphasis is placed on the theoretical fundamentals of designing self-test VLSI building blocks, such as built-in test generators and output response analyzers. Particular attention is paid to: structural design of self-test VLSI circuits; design of universal modules for self-test VLSI circuits; and examination of the VLSI

circuits for signature testability. It has been demonstrated that the design-for-testability techniques employed by this method provide ideal conditions for the straightforward implementation of self-test concepts. The work should prove useful for all those interested in both the basic facts and current research in this field.

Computers, Software Engineering, and Digital Devices Springer Science & Business Media
Using the book and the software provided with it, the reader can build his/her own tester arrangement to investigate key aspects of analog-, digital- and mixed system circuits
Plan of attack based on traditional testing, circuit design and circuit manufacture allows the reader to appreciate a testing regime from the point of view of all the participating interests
Worked examples based on theoretical bookwork, practical experimentation and simulation exercises teach the reader how to test circuits thoroughly and effectively
John Wiley & Sons
Last, but not least, thanks to all the participants and authors. We hope that they enjoyed the workshop as much as the wonderful and culturally vibrant city of Kolkata! Bhabani P. Sinha Indian Statistical Institute, Kolkata, India December 2004 Sajal K. Das University of Texas, Arlington, USA December 2004 Program Chairs' Message On behalf of the Technical Program Committee of the 6th International Wo- shop on Distributed Computing, IWDC 2004, it was our great pleasure to w- come the attendees to Kolkata, India. Over the last few years, IWDC has emerged as an internationally renowned forum for interaction among researchers from academia and industries around the world. A clear indicator of this fact is the large number of high-quality submissions of technical papers received by the workshop this year. The workshop program consisted of 12 technical sessions with 54 contributed papers, two keynote addresses, four tutorials, a panel, a poster session and the Prof.A.K.ChoudhuryMemorialLecture.TheIWDCProgramCommittee,c- prising 38 distinguished members, worked hard to organize the technical p- gram. Following a rigorous review process, out of 157 submissions only 54 - pers were accepted for presentation in the technical sessions; 27 of the accepted papers were classi?ed as regular papers and the remaining 27 as short papers. Another 11 papers were accepted for presentation in the poster session, each with a one-page abstract appearing in the proceedings.

IDDQ Testing of VLSI Circuits Springer Nature
This handbook provides ready access to all of the major concepts, techniques, problems, and solutions in the emerging field of pseudorandom pattern testing. Until now, the literature in this area has been widely scattered, and published work, written by professionals in several disciplines, has treated notation and mathematics in ways that vary from source to source. This book opens with a clear description of the shortcomings of conventional testing as applied to complex digital circuits, revewing by comparison the principles of design for testability of more advanced digital technology. Offers in-depth discussions of test sequence generation and response data

compression, including pseudorandom sequence generators; the mathematics of shift-register sequences and their potential for built-in testing. Also details random and memory testing and the problems of assessing the efficiency of such tests, and the limitations and practical concerns of built-in testing.

Economics of Electronic Design, Manufacture and Test Built In Test for VLSI The general understanding of design is that it should lead to a manufacturable product. Neither the design nor the process of manufacturing is perfect. As a result, the product will be faulty, will require testing and fixing. Where does economics enter this scenario? Consider the cost of testing and fixing the product. If a manufactured product is grossly faulty, or too many of the products are faulty, the cost of testing and fixing will be high. Suppose we do not like that. We then ask what is the cause of the faulty product. There must be something wrong in the manufacturing process. We trace this cause and fix it. Suppose we fix all possible causes and have no defective products. We would have eliminated the need for testing. Unfortunately, things are not so perfect. There is a cost involved with finding and eliminating the causes of faults. We thus have two costs: the cost of testing and fixing (we will call it cost-1), and the cost of finding and eliminating causes of faults (call it cost-2). Both costs, in some way, are included in the overall cost of the product. If we try to eliminate cost-1, cost-2 goes up, and vice versa. An economic system of production will minimize the overall cost of the product. Economics of Electronic Design, Manufacture and Test is a collection of research contributions derived from the Second Workshop on Economics of Design, Manufacture and Test, written for inclusion in this book.

Fachgespräche auf der 14. GI-Jahrestagung IET Power supply current monitoring to detect CMOS IC defects during production testing quietly laid down its roots in the mid-1970s. Both Sandia Labs and RCA in the United States and Philips Labs in the Netherlands practiced this procedure on their CMOS ICs. At that time, this practice stemmed simply from an intuitive sense that CMOS ICs showing abnormal quiescent power supply current (IDDQ) contained defects. Later, this intuition was supported by data and analysis in the 1980s by Levi (RACD, Malaiya and Su (SUNY-Binghamton), Soden and Hawkins (Sandia Labs and the University of New Mexico), Jacomino and co-workers (Laboratoire d'Automatique de Grenoble), and Maly and co-workers (Carnegie Mellon University). Interest in IDDQ testing has advanced beyond the data reported in the 1980s and is now focused on applications and evaluations involving larger volumes of ICs that improve quality beyond what can be achieved by previous conventional means. In the conventional style of testing one attempts to propagate the logic states of the suspended nodes to primary outputs. This is done for all or most nodes of the circuit. For sequential circuits, in particular, the complexity of finding suitable tests is very high. In comparison, the IDDQ test does not observe the logic states, but measures the integrated current that leaks through all gates. In other words, it is like

measuring a patient's temperature to determine the state of health. Despite perceived advantages, during the years that followed its initial announcements, skepticism about the practicality of IDDQ testing prevailed. The idea, however, provided a great opportunity to researchers. New results on test generation, fault simulation, design for testability, built-in self-test, and diagnosis for this style of testing have since been reported. After a decade of research, we are definitely closer to practice.

Built In Test for VLSI
Prentice Hall
This book discusses the new roles that the VLSI (very-large-scale integration of semiconductor circuits) is taking for the safe, secure, and dependable design and operation of electronic systems. The book consists of three parts. Part I, as a general introduction to this vital topic, describes how electronic systems are designed and tested with particular emphasis on dependability engineering, where the simultaneous assessment of the detrimental outcome of failures and cost of their containment is made. This section also describes the related research project "Dependable VLSI Systems," in which the editor and authors of the book were involved for 8 years. Part II addresses various threats to the dependability of VLSIs as key systems components, including time-dependent degradations, variations in device characteristics, ionizing radiation, electromagnetic interference, design errors, and tampering, with discussion of technologies to counter those threats. Part III elaborates on the design and test technologies for dependability in such applications as control of robots and vehicles, data processing, and storage in a cloud environment and heterogeneous wireless telecommunications. This book is intended to be used as a reference for engineers who work on the design and testing of VLSI systems with particular attention to dependability. It can be used as a textbook in graduate courses as well. Readers interested in dependable systems from social and industrial–economic perspectives will also benefit from the discussions in this book.

VLSI Design and Test for Systems Dependability
Springer Science & Business Media
The idea of creating the European Dependable Computing Conference (EDCC) was born at the moment when the Iron Curtain fell. A group of enthusiasts, who were pre viously involved in research and teaching in the ?eld of fault tolerant computing in different European countries, agreed that there is no longer any point in keeping pre viously independent activities apart and created a steering committee which took the responsibility for preparing the EDCC calendar and appointing the chairs for the in dividual conferences. There is no single European or global professional organization that took over the responsibility for this conference, but there are three national in terest groups that sent delegates to the steering committee and support its activities, especially by promoting the conference materials. As can be seen from these materi als, they are the SEE Working Group "Dependable Computing" (which is a successor organizationof AFCET)in

France,theGI/ITG/GMATechnicalCommitteeonDependability and Fault Tolerance in Germany, and the AICA Working Group “Dependability of Computer Systems” in Italy. In addition, committees of several global professional organizations, such as IEEE and IFIP, support this conference. Prague has been selected as a conference venue for several reasons. It is an easily accessible location that may attract many visitors by its beauty and that has a tradition in organizing international events of this kind (one of the last FTSD conferences took place here).