Esd Basics From Semiconductor Manufacturing To Product Use

ESD Protection Device and Circuit Design for Advanced CMOS Technologies
An Engineer's Guide to Automated Testing of High-Speed Interfaces, Second Edition
Concepts, Methodologies, Tools, and Applications
Devices, Circuits and Systems
ESD Basics
Contamination and ESD Control in High-Technology Manufacturing
A State of the Art Handbook, Volume 1
Planning Production and Inventories in the Extended Enterprise
Materials Science and Engineering: Concepts, Methodologies, Tools, and Applications
Electrical Overstress (EOS)
Circuits and Devices
The ESD Control Program Handbook
Bits on Chips
Principles and Applications in Cleanroom Automation
Handbook of Semiconductor Manufacturing Technology

Robotics for Electronics Manufacturing
ESD Design for Analog Circuits
Design and Synthesis
ESD Testing
Integrated Circuit Design for Radiation Environments
Electrostatic Discharge
U.S. Regulation of the International Securities and Derivatives Markets
Physics and Devices
ESD Design and Analysis Handbook
The ESD Handbook
Research Perspectives on Functional Micro- and Nanoscale Coatings
ESD
Series on Emission Scenario Documents Photoresist Use in Semiconductor Manufacturing
Low-Power Electronics Design
Transient-Induced Latchup in CMOS Integrated Circuits
From Semiconductor Manufacturing to Product Use
ESD in Silicon Integrated Circuits
System Level ESD Co-Design
Low-Power CMOS Circuits

ESD Products and Materials
Technology, Logic Design and CAD Tools
ESD
Product Lifecycle Management (Volume 1)

REAGAN DRAVEN

ESD Protection Device and Circuit Design for Advanced CMOS Technologies Springer Science & Business Media In two volumes, Planning Production and Inventories in the Extended Enterprise: A State of the Art Handbook examines production planning across the extended enterprise against a backdrop of important gaps between theory and practice. The early chapters describe the multifaceted nature of production planning problems and reveal many of the core complexities. The middle chapters describe recent research on theoretical techniques to manage these complexities. Accounts of production planning system currently in use in various industries are included in the later chapters. Throughout the two volumes there are suggestions on promising directions for future work focused on closing the gaps.
An Engineer's Guide to Automated Testing of High-Speed Interfaces,

Second Edition Aspen Publishers
The book all semiconductor device engineers must read to gain a practical feel for latchup-induced failure to produce lower-cost and higher-density chips. Transient-Induced Latchup in CMOS Integrated Circuits equips the practicing engineer with all the tools needed to address this regularly occurring problem while becoming more proficient at IC layout. Ker and Hsu introduce the phenomenon and basic physical mechanism of latchup, explaining the critical issues that have resurfaced for CMOS technologies. Once readers can gain an understanding of the standard practices for TLU, Ker and Hsu discuss the physical mechanism of TLU under a system-level ESD test, while introducing an efficient component-level TLU measurement setup. The authors then present experimental methodologies to extract safe and area-efficient compact layout rules for latchup prevention, including layout rules for I/O cells, internal circuits, and between I/O and internal circuits. The book concludes with an appendix giving a practical example of extracting layout rules and guidelines for latchup prevention in a 0.18-micrometer 1.8V/3.3V silicided CMOS process. Presents real cases and solutions that occur in commercial CMOS IC chips Equips engineers with the skills to conserve chip layout area and decrease time-to-market

Written by experts with real-world experience in circuit design and failure analysis Distilled from numerous courses taught by the authors in IC design houses worldwide The only book to introduce TLU under system-level ESD and EFT tests This book is essential for practicing engineers involved in IC design, IC design management, system and application design, reliability, and failure analysis. Undergraduate and postgraduate students, specializing in CMOS circuit design and layout, will find this book to be a valuable introduction to real-world industry problems and a key reference during the course of their careers.

Concepts, Methodologies, Tools, and Applications IGI Global

ESD Protection Device and Circuit Design for Advanced CMOS Technologies is intended for practicing engineers working in the areas of circuit design, VLSI reliability and testing domains. As the problems associated with ESD failures and yield losses become significant in the modern semiconductor industry, the demand for graduates with a basic knowledge of ESD is also increasing. Today, there is a significant demand to educate the circuits design and reliability teams on ESD issues. This book makes an attempt to address the ESD design and implementation in a systematic manner. A design procedure involving device simulators as well as circuit simulator is employed to optimize

device and circuit parameters for optimal ESD as well as circuit performance. This methodology, described in ESD Protection Device and Circuit Design for Advanced CMOS Technologies has resulted in several successful ESD circuit design with excellent silicon results and demonstrates its strengths.

Devices, Circuits and Systems John Wiley & Sons

An effective and cost efficient protection of electronic system against ESD stress pulses specified by IEC 61000-4-2 is paramount for any system design. This pioneering book presents the collective knowledge of system designers and system testing experts and state-of-the-art techniques for achieving efficient system-level ESD protection, with minimum impact on the system performance. All categories of system failures ranging from 'hard' to 'soft' types are considered to review simulation and tool applications that can be used. The principal focus of System Level ESD Co-Design is defining and establishing the importance of co-design efforts from both IC supplier and system builder perspectives. ESD designers often face challenges in meeting customers' system-level ESD requirements and, therefore, a clear understanding of the techniques presented here will facilitate effective simulation approaches leading to better solutions without

compromising system performance. With contributions from Robert Ashton, Jeffrey Dunnihoo, Micheal Hopkins, Pratik Maheshwari, David Pomerenke, Wolfgang Reinprecht, and Matti Usumaki, readers benefit from hands-on experience and in-depth knowledge in topics ranging from ESD design and the physics of system ESD phenomena to tools and techniques to address soft failures and strategies to design ESD-robust systems that include mobile and automotive applications.

The first dedicated resource to system-level ESD co-design, this is an essential reference for industry ESD designers, system builders, IC suppliers and customers and also Original Equipment Manufacturers (OEMs). Key features: Clarifies the concept of system level ESD protection. Introduces a co-design approach for ESD robust systems. Details soft and hard ESD fail mechanisms. Detailed protection strategies for both mobile and automotive applications.

Explains simulation tools and methodology for system level ESD co-design and overviews available test methods and standards. Highlights economic benefits of system ESD co-design. John Wiley & Sons Electrostatic discharge (ESD) continues to impact semiconductor components and systems as technologies scale from micro- to nano-electronics. This book studies electrical overstress, ESD, and latchup from a whole-chip ESD design synthesis

approach. It provides a clear insight into the integration of ESD protection networks from a generalist perspective, followed by examples in specific technologies, circuits, and chips. Uniquely both the semiconductor chip integration issues and floorplanning of ESD networks are covered from a ‘top-down' design approach. Look inside for extensive coverage on: integration of cores, power bussing, and signal pins in DRAM, SRAM, CMOS image processing chips, microprocessors, analog products, RF components and how the integration influences ESD design and integration architecturing of mixed voltage, mixed signal, to RF design for ESD analysis floorplanning for peripheral and core I/O designs, and the implications on ESD and latchup guard ring integration for both a ‘bottom-up' and ‘top-down' methodology addressing I/O guard rings, ESD guard rings, I/O to I/O, and I/O to core classification of ESD power clamps and ESD signal pin circuitry, and how to make the correct choice for a given semiconductor chip examples of ESD design for the state-of-the-art technologies discussed, including CMOS, BiCMOS, silicon on insulator (SOI), bipolar technology, high voltage CMOS (HVCMOS), RF CMOS, and smart power practical methods for the understanding of ESD circuit power distribution, ground rule development, internal bus distribution, current path analysis, quality metrics

ESD: Design and Synthesis is a continuation of the author's series of books on ESD protection. It is an essential reference for: ESD, circuit, and semiconductor engineers; design synthesis team leaders; layout design, characterisation, floorplanning, test and reliability engineers; technicians; and groundrule and test site developers in the manufacturing and design of semiconductor chips. It is also useful for graduate and undergraduate students in electrical engineering, semiconductor sciences, and manufacturing sciences, and on courses involving the design of ESD devices, chips and systems. This book offers a useful insight into the issues that confront modern technology as we enter the nano-electronic era.

ESD Basics John Wiley & Sons

Electrostatic discharge (ESD) is defined as the transfer of charge between bodies at different potentials. The electrostatic discharge induced integrated circuit damages occur throughout the whole life of a product from the manufacturing, testing, shipping, handing, to end user operating stages. This is particularly true as microelectronics technology continues shrink to nano-metric dimensions. The ESD related failures is a major IC reliability concern and results in a loss of millions dollars to the semiconductor industry each year. Several ESD stress models and test

methods have been developed to reproduce the real world ESD discharge events and quantify the sensitivity of ESD protection structures. The basic ESD models are: Human body model (HBM), Machine model (MM), and Charged device model (CDM). To avoid or reduce the IC failure due to ESD, the on-chip ESD protection structures and schemes have been implemented to discharge ESD current and clamp overstress voltage under different ESD stress events. Because of its simple structure and good performance, the junction diode is widely used in on-chip ESD protection applications. This is particularly true for ESD protection of low-voltage ICs where a relatively low trigger voltage for the ESD protection device is required. However, when the diode operates under the ESD stress, its current density and temperature are far beyond the normal conditions and the device is in danger of being damaged. For the design of effective ESD protection solution, the ESD robustness and low parasitic capacitance are two major concerns. The ESD robustness is usually defined after the failure current It2 and on-state resistance Ron. The transmission line pulsing (TLP) measurement is a very effective tool for evaluating the ESD robustness of a circuit or single element. This is particularly helpful in characterizing the effect of HBM stress where the ESD-induced damages are more likely due to thermal failures. Two types of diodes with different

anode/cathode isolation technologies will be investigated for their ESD performance: one with a LOCOS (Local Oxidation of Silicon) oxide isolation called the LOCOS-bound diode, the other with a polysilicon gate isolation called the polysilicon-bound diode. We first examine the ESD performance of the LOCOS-bound diode. The effects of different diode geometries, metal connection patterns, dimensions and junction configurations on the ESD robustness and parasitic capacitance are investigated experimentally. The devices considered are N+/P-well junction LOCOS-bound diodes having different device widths, lengths and finger numbers, but the approach applies generally to the P+/N-well junction diode as well. The results provide useful insights into optimizing the diode for robust HBM ESD protection applications. Then, the current carrying and voltage clamping capabilities of LOCOS- and polysilicon-bound diodes are compared and investigated based on both TCAD simulation and experimental results. Comparison of these capabilities leads to the conclusion that the polysilicon-bound diode is more suited for ESD protection applications due to its higher performance. The effects of polysilicon-bound diode's design parameters, including the device width, anode/cathode length, finger number, poly-gate length, terminal

connection and metal topology, on the ESD robustness are studied. Two figures of merits, FOM_It2 and FOM_Ron, are developed to better assess the effects of different parameters on polysilicon-bound diode's overall ESD performance. As latest generation package styles such as mBGAs, SOTs, SC70s, and CSPs are going to the millimeter-range dimensions, they are often effectively too small for people to handle with fingers. The recent industry data indicates the charged device model (CDM) ESD event becomes increasingly important in today's manufacturing environment and packaging technology. This event generates highly destructive pulses with a very short rise time and very small duration. TLP has been modified to probe CDM ESD protection effectiveness. The pulse width was reduced to the range of 1-10 ns to mimic the very fast transient of the CDM pulses. Such a very fast TLP (VFTLP) testing has been used frequently for CDM ESD characterization. The overshoot voltage and turn-on time are two key considerations for designing the CDM ESD protection devices. A relatively high overshoot voltage can cause failure of the protection devices as well as the protected devices, and a relatively long turn-on time may not switch on the protection device fast enough to effectively protect the core circuit against the CDM stress. The overshoot voltage and turn-on time of an ESD

protection device can be observed and extracted from the voltage versus time waveforms measured from the VFTLP testing. Transient behaviors of polysilicon-bound diodes subject to pulses generated by the VFTLP tester are characterized for fast ESD events such as the charged device model. The effects of changing devices' dimension parameters on the transient behaviors and on the overshoot voltage and turn-on time are studied. The correlation between the diode failure and poly-gate configuration under the VFTLP stress is also investigated. Silicon-controlled rectifier (SCR) is another widely used ESD device for protecting the I/O pins and power supply rails of integrated circuits. Multiple fingers are often needed to achieve optimal ESD protection performance, but the uniformity of finger triggering and current flow is always a concern for multi-finger SCR devices operating under the post-snapback region. Without a proper understanding of the finger turn-on mechanism, design and realization of robust SCRs for ESD protection applications are not possible. Two two-finger SCRs with different combinations of anode/cathode regions are considered, and their finger turn-on uniformities are analyzed based on the I-V characteristics obtained from the transmission line pulsing (TLP) tester. The dV/dt effect of pulses with different rise times on the finger turn-on behavior of

the SCRs are also investigated experimentally. In this work, unless noted otherwise, all the measurements are conducted using the Barth 4002 transmission line pulsing (TLP) and Barth 4012 very-fast transmission line pulsing (VFTLP) testers.

Contamination and ESD Control in High-Technology Manufacturing ESD BasicsFrom Semiconductor Manufacturing to Product Use

ESD BasicsFrom Semiconductor Manufacturing to Product UseJohn Wiley & Sons

A State of the Art Handbook, Volume 1 Springer Nature

A practical guide to the effects of radiation on semiconductor components of electronic systems, and techniques for the designing, laying out, and testing of hardened integrated circuits This book teaches the fundamentals of radiation environments and their effects on electronic components, as well as how to design, lay out, and test cost-effective hardened semiconductor chips not only for today's space systems but for commercial terrestrial applications as well. It provides a historical perspective, the fundamental science of radiation, and the basics of semiconductors, as well as radiation-induced failure mechanisms in semiconductor chips. Integrated Circuits Design for Radiation Environments starts by introducing readers to

semiconductors and radiation environments (including space, atmospheric, and terrestrial environments) followed by circuit design and layout. The book introduces radiation effects phenomena including single-event effects, total ionizing dose damage and displacement damage) and shows how technological solutions can address both phenomena. Describes the fundamentals of radiation environments and their effects on electronic components Teaches readers how to design, lay out and test cost-effective hardened semiconductor chips for space systems and commercial terrestrial applications Covers natural and man-made radiation environments, space systems and commercial terrestrial applications Provides up-to-date coverage of state-of-the-art of radiation hardening technology in one concise volume Includes questions and answers for the reader to test their knowledge Integrated Circuits Design for Radiation Environments will appeal to researchers and product developers in the semiconductor, space, and defense industries, as well as electronic engineers in the medical field. The book is also helpful for system, layout, process, device, reliability, applications, ESD, latchup and circuit design semiconductor engineers, along with anyone involved in micro-electronics used in harsh environments.

Planning Production and Inventories in the

Extended Enterprise
Artech House
The power consumption of integrated circuits is one of the most problematic considerations affecting the design of high-performance chips and portable devices. The study of power-saving design methodologies now must also include subjects such as systems on chips, embedded software, and the future of microelectronics. Low-Power Electronics Design covers all major aspects of low-power design of ICs in deep submicron technologies and addresses emerging topics related to future design. This volume explores, in individual chapters written by expert authors, the many low-power techniques born during the past decade. It also discusses the many different domains and disciplines that impact power consumption, including processors, complex circuits, software, CAD tools, and energy sources and management. The authors delve into what many specialists predict about the future by presenting techniques that are promising but are not yet reality. They investigate nanotechnologies, optical circuits, ad hoc networks, e-textiles, as well as human powered sources of energy. Low-Power Electronics Design delivers a complete picture of today's methods for reducing power, and also illustrates the advances in chip design that may be commonplace 10 or 15 years from now.
Materials Science and Engineering: Concepts,

Methodologies, Tools, and Applications John Wiley & Sons
"Electrostatic discharge (ESD)"--Page xxi.
Electrical Overstress (EOS) Springer Science & Business Media
Electrostatic Discharge is a pervasive issue in the semiconductor industry affecting both manufacturers and users of semiconductors. This easy-to-read, practical handbook presents an overview of ESD as it effects electronic circuits and provides a concise introduction for students, engineers, circuit designers and failure analysts.
Circuits and Devices John Wiley & Sons
* Examines the various methods available for circuit protection, including coverage of the newly developed ESD circuit protection schemes for VLSI circuits. * Provides guidance on the implementation of circuit protection measures. * Includes new sections on ESD design rules, layout approaches, package effects, and circuit concepts. * Reviews the new Charged Device Model (CDM) test method and evaluates design requirements necessary for circuit protection.
The ESD Control Program Handbook Springer
This Book and Simulation Software Bundle Project Dear Reader, this book project brings to you a unique study tool for ESD protection solutions used in analog-integrated circuit (IC) design. Quick-start learning is combined with in-depth understanding for the whole spectrum of cro-disciplinary knowledge

required to excel in the ESD ?eld. The chapters cover technical material from elementary semiconductor structure and device levels up to complex analog circuit design examples and case studies. The book project provides two different options for learning the material. The printed material can be studied as any regular technical textbook. At the same time, another option adds parallel exercise using the trial version of a complementary commercial simulation tool with prepared simulation examples. Combination of the textbook material with numerical simulation experience presents a unique opportunity to gain a level of expertise that is hard to achieve otherwise. The book is bundled with simpli?ed trial version of commercial mixed- TM mode simulation software from Angstrom Design Automation. The DECIMM (Device Circuit Mixed-Mode) simulator tool and complementary to the book s- ulation examples can be downloaded from www.analogesd.com. The simulation examples prepared by the authors support the speci?c examples discussed across the book chapters. A key idea behind this project is to provide an opportunity to not only study the book material but also gain a much deeper understanding of the subject by direct experience through practical simulation examples.

Bits on Chips John Wiley & Sons

This book provides

readers with a broad overview of integrated circuits, also generally referred to as micro-electronics. The presentation is designed to be accessible to readers with limited, technical knowledge and coverage includes key aspects of integrated circuit design, implementation, fabrication and application. The author complements his discussion with a large number of diagrams and photographs, in order to reinforce the explanations. The book is divided into two parts, the first of which is specifically developed for people with almost no or little technical knowledge. It presents an overview of the electronic evolution and discusses the similarity between a chip floor plan and a city plan, using metaphors to help explain concepts. It includes a summary of the chip development cycle, some basic definitions and a variety of applications that use integrated circuits. The second part digs deeper into the details and is perfectly suited for professionals working in one of the semiconductor disciplines who want to broaden their semiconductor horizon.

Principles and Applications in Cleanroom Automation

IGI Global

This second edition of An Engineer's Guide to Automated Testing of High-Speed Interfaces provides updates to reflect current state-of-the-art high-speed digital testing with automated test equipment

technology (ATE). Featuring clear examples, this one-stop reference covers all critical aspects of automated testing, including an introduction to high-speed digital basics, a discussion of industry standards, ATE and bench instrumentation for digital applications, and test and measurement techniques for characterization and production environment. Engineers learn how to apply automated test equipment for testing high-speed digital I/O interfaces and gain a better understanding of PCI-Express 4, 100Gb Ethernet, and MIPI while exploring the correlation between phase noise and jitter. This updated resource provides expanded material on 28/32 Gbps NRZ testing and wireless testing that are becoming increasingly more pertinent for future applications. This book explores the current trend of merging high-speed digital testing within the fields of photonic and wireless testing.

Handbook of Semiconductor Manufacturing Technology

BoD – Books on Demand

As we enter the nanoelectronics era, electrostatic discharge (ESD) phenomena is an important issue for everything from micro-electronics to nanostructures. This book provides insight into the operation and design of micro-gaps and nanogenerators with chapters on low capacitance ESD design in advanced technologies, electrical breakdown in micro-gaps, nanogenerators from ESD,

and theoretical prediction and optimization of triboelectric nanogenerators. The information contained herein will prove useful for for engineers and scientists that have an interest in ESD physics and design.

Robotics for Electronics Manufacturing Springer

A comprehensive and in-depth review of analog circuitlayout, schematic architecture, device, power network and ESDdesign This book will provide a balanced overview of analog circuitdesign layout, analog circuit schematic development,architecture of chips, and ESD design. It will start atan introductory level and will bring the reader right up to thestate-of-the-art. Two critical design aspects for analog and powerintegrated circuits are combined. The first design aspect coversanalog circuit design techniques to achieve the desired circuitperformance. The second and main aspect presents the additionalchallenges associated with the design of adequate and effective ESDprotection elements and schemes. A comprehensive list of practicalapplication examples is used to demonstrate the successfulcombination of both techniques and any potential designtrade-offs. Chapter One looks at analog design discipline, including layoutand analog matching and analog layout design practices. Chapter Twodiscusses analog design with circuits, examining:

singletransistor amplifiers; multi-transistor amplifiers; active loadsand more. The third chapter covers analog design layout (alsoMOSFET layout), before Chapters Four and Five discuss analog designsynthesis. The next chapters introduce the reader to analog-digitalmixed signal design synthesis, analog signal pin ESD networks, andanalog ESD power clamps. Chapter Nine, the last chapter, covers ESDdesign in analog applications. Clearly describes analog design fundamentals (circuitfundamentals) as well as outlining the various ESDimplications Covers a large breadth of subjects and technologies, such asCMOS, LDMOS, BCD, SOI, and thick body SOI Establishes an “ESD analog design” discipline thatdistinguishes itself from the alternative ESD digital designfocus Focuses on circuit and circuit design applications Assessible, with the artwork and tutorial style of the ESD bookseries PowerPoint slides are available for university facultymembers Even in the world of digital circuits, analog and power circuitsare two very important but under-addressed topics, especially fromthe ESD aspect. Dr. Voldman’s new book will serve as anessential and practical guide to the greater IC community. Withhigh practical and academic values this book is a“bible” for professionals, graduate students, deviceand circuit designers for investigating the physics of ESD and forproduct

designs and testing. *ESD Design for Analog Circuits* John Wiley & Sons A practical and comprehensive reference that explores Electrostatic Discharge (ESD) in semiconductor components and electronic systems The ESD Handbook offers a comprehensive reference that explores topics relevant to ESD design in semiconductor components and explores ESD in various systems. Electrostatic discharge is a common problem in the semiconductor environment and this reference fills a gap in the literature by discussing ESD protection. Written by a noted expert on the topic, the text offers a topic-by-topic reference that includes illustrative figures, discussions, and drawings. The handbook covers a wide-range of topics including ESD in manufacturing (garments, wrist straps, and shoes); ESD Testing; ESD device physics; ESD semiconductor process effects; ESD failure mechanisms; ESD circuits in different technologies (CMOS, Bipolar, etc.); ESD circuit types (Pin, Power, Pin-to-Pin, etc.); and much more. In addition, the text includes a glossary, index, tables, illustrations, and a variety of case studies. Contains a well-organized reference that provides a quick review on a range of ESD topics Fills the gap in the current literature by providing information from purely scientific and physical aspects to practical applications Offers information in clear and accessible terms Written by the accomplished author of

the popular ESD book series Written for technicians, operators, engineers, circuit designers, and failure analysis engineers, The ESD Handbook contains an accessible reference to ESD design and ESD systems.

Design and Synthesis CRC Press

This OECD Emission Scenario Document (ESD) provides information on the sources, use patterns, and potential release pathways of chemicals used in the semiconductor manufacturing industry.

ESD Testing John Wiley & Sons

Electrical Overstress (EOS) continues to impact semiconductor manufacturing, semiconductor components and systems as technologies scale from micro- to nano-electronics. This bookteaches the fundamentals of electrical overstress and how to minimize and mitigate EOS failures. The text provides a clear picture of EOS phenomena, EOS origins, EOS sources, EOS physics, EOS failure mechanisms, and EOS on-chip and system design. It provides an illuminating insight into the sources of EOS in manufacturing, integration of on-chip, and system level EOS protection networks, followed by examples in specific technologies, circuits, and chips. The book is unique in covering the EOS manufacturing issues from on-chip design and electronic design automation to factory-level EOS program management in today’s modern world. Look inside for extensive coverage

on: Fundamentals of electrical overstress, from EOS physics, EOS time scales, safe operating area (SOA), to physical models for EOS phenomena EOS sources in today's semiconductor manufacturing environment, and EOS program management, handling and EOS auditing processing to avoid EOS failures EOS failures in both semiconductor devices, circuits and system Discussion of how to distinguish between EOS events, and electrostatic discharge (ESD) events (e.g. such as human body model (HBM), charged device model (CDM), cable discharge events (CDM), charged board events (CBE), to system level IEC 61000-4-2 test events) EOS protection on-chip design practices and how they differ from ESD protection networks and solutions Discussion of EOS system level concerns in printed circuit boards (PCB), and manufacturing equipment Examples of EOS issues in state-of-the-art digital, analog and power technologies including CMOS, LDMOS, and BCD EOS design rule checking (DRC), LVS, and ERC electronic design automation (EDA) and how it is distinct from ESD EDA systems EOS testing and qualification techniques, and Practical off-chip ESD protection and system level solutions to provide more robust systems Electrical Overstress (EOS): Devices, Circuits and Systems is a continuation of the author's series of books on ESD protection. It is an essential reference

and a useful insight into modern technology as we enter the nano-electronic era.

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