Digital Integrated Circuits Jan M Rabaey

Progress in Cryptology – INDOCRYPT 2007
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Multi-Core Embedded Systems
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Digitally-Assisted Analog and Analog-Assisted Digital IC Design
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MIMO Systems
TFET Integrated Circuits
Power Analysis Attacks
Ultra-Low Power Integrated Circuit Design
Digital VLSI Chip Design with Cadence and Synopsys CAD Tools

Electronics, Communications and Networks IV
FPGA Hardware-Entwurf
Power Aware Design Methodologies
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Proceedings of Seventh International Conference on Bio-Inspired Computing: Theories and Applications (BIC-TA 2012)
Design, Manufacturing And Mechatronics - Proceedings Of The International Conference On Design, Manufacturing And Mechatronics (Icdmm2016)
Digital Integrated Circuits
Low Power Design Essentials
A System Study for RFID
Digital Integrated Circuits
Low Power Interconnect Design
Design of High Voltage xDSL Line Drivers in Standard CMOS
Integrated Circuit and System Design

HOUSTON CAROLYN

Progress in Cryptology – INDOCRYPT 2007 Prentice Hall
This volume covers a wide area ? from research topics to the design and improvement of integrated circuit devices, already existing or to be introduced to the market.
Entwurf von digitalen Schaltungen und Systemen mit HDLs und FPGAs CRC Press
Details a real-world product that applies a cutting-edge multi-core architecture Increasingly demanding modern applications—such as those used in telecommunications networking and real-time processing of audio, video, and multimedia streams—require multiple processors to achieve computational performance at the rate of a few giga-operations per second. This necessity for speed and manageable power consumption makes it likely that the next generation of embedded processing systems will include hundreds of cores, while being increasingly programmable, blending processors and configurable hardware in a power-efficient manner. Multi-Core Embedded Systems presents a variety of perspectives that elucidate the technical challenges associated with such increased integration of homogeneous (processors) and heterogeneous multiple cores. It offers an analysis that industry engineers and professionals will need to understand the physical details of both software and hardware in embedded architectures, as well as their limitations and potential for future growth. Discusses the available programming models

spread across different abstraction levels The book begins with an overview of the evolution of multiprocessor architectures for embedded applications and discusses techniques for autonomous power management of system-level parameters. It addresses the use of existing open-source (and free) tools originating from several application domains—such as traffic modeling, graph theory, parallel computing and network simulation. In addition, the authors cover other important topics associated with multi-core embedded systems, such as: Architectures and interconnects Embedded design methodologies Mapping of applications

Digital Integrated Circuit Design Springer Science & Business Media

This book presents Dual Mode Logic (DML), a new design paradigm for digital integrated circuits. DML logic gates can operate in two modes, each optimized for a different metric. Its on-the-fly switching between these operational modes at the gate, block and system levels provide maximal E-D optimization flexibility. Each highly detailed chapter has multiple illustrations showing how the DML paradigm seamlessly implements digital circuits that dissipate less energy while simultaneously improving performance and reducing area without a significant compromise in reliability. All the facets of the DML methodology are covered, starting from basic concepts, through single gate optimization, general module optimization, design trade-offs and new ways DML can be integrated into standard design flows using standard EDA tools. DML logic is compatible with numerous applications but is particularly advantageous for ultra-low power, reliable high performance systems, and advanced scaled technologies Written in language accessible to students and design engineers, each topic is oriented toward immediate application by all those interested in an alternative to CMOS logic. Describes a novel, promising alternative to conventional CMOS logic, known as Dual Mode Logic (DML), with which a single gate can be operated selectively in two modes, each optimized for a different metric (e.g., energy consumption, performance, size); Demonstrates several techniques at the architectural level, which can result in high energy savings and improved system performance; Focuses on the tradeoffs between power, area and speed including optimizations at the transistor and gate level, including alternatives to DML basic cells; Illustrates DML efficiency for a variety of VLSI applications.

Polymers in Organic Electronics World Scientific

Discover cutting-edge techniques for next-generation integrated circuit design, and learn how to deliver improved speed, density, power, and cost.

Circadian Rhythms for Future Resilient Electronic Systems Cambridge University Press

Power Aware Design Methodologies was conceived as an effort to bring all aspects of power-aware design methodologies together in a single document. It covers several layers of the design hierarchy from technology, circuit logic, and architectural levels up to the system layer. It includes discussion of techniques and methodologies for improving the power efficiency of CMOS circuits (digital and analog), systems on chip, microelectronic systems, wirelessly networked systems of computational nodes and so on. In addition to providing an in-depth analysis of the sources of power dissipation in VLSI circuits and systems and the

technology and design trends, this book provides a myriad of state-of-the-art approaches to power optimization and control. The different chapters of Power Aware Design Methodologies have been written by leading researchers and experts in their respective areas. Contributions are from both academia and industry. The contributors have reported the various technologies, methodologies, and techniques in such a way that they are understandable and useful.

Modern VLSI Design Springer Science & Business Media

This book describes the physical operation of the Tunnel Field-effect Transistor (TFET) and circuits built with this device. Whereas the majority of publications on TFETs describe in detail the device, its characteristics, variants and performance, this will be the first book addressing TFET integrated circuits (TFET ICs). The authors describe the peculiarities of TFET ICs and their differences with MOSFETs. They also develop and analyze a number of logic circuits and memories. The discussion also includes complex circuits combining CMOS and TFET, as well as a potential fabrication process in Silicon.

Dual Mode Logic Springer Science & Business Media

This book describes methods to address wearout/aging degradations in electronic chips and systems, caused by several physical mechanisms at the device level. The authors introduce a novel technique called accelerated active self-healing, which fixes wearout issues by enabling accelerated recovery. Coverage includes recovery theory, experimental results, implementations and applications, across multiple nodes ranging from planar, FD-SOI to FinFET, based on both foundry provided models and predictive models. Presents novel techniques, tested with experiments on real hardware; Discusses circuit and system level wearout recovery implementations, many of these designs are portable and friendly to the standard design flow; Provides circuit-architecture-system infrastructures that enable the accelerated self-healing for future resilient systems; Discusses wearout issues at both transistor and interconnect level, providing solutions that apply to both; Includes coverage of resilient aspects of emerging applications such as IoT.

Current Sense Amplifiers for Embedded SRAM in High-Performance System-on-a-Chip Designs Elsevier

This practical, tool-independent guide to designing digital circuits takes a unique, top-down approach, reflecting the nature of the design process in industry. Starting with architecture design, the book comprehensively explains the why and how of digital circuit design, using the physics designers need to know, and no more.

CRC Press

The 4th International Conference on Electronic, Communications and Networks (CECNet2014) inherits the fruitfulness of the past three conferences and lays a foundation for the forthcoming next year in Shanghai. CECNet2014 was hosted by Hubei University of Science and Technology, China, with the main objective of providing a comprehensive global foru

Berkshire Encyclopedia of Sustainability 7/10 Springer Science & Business Media

Intended for use in undergraduate senior-level digital circuit design courses with advanced material sufficient for graduate-level courses. Progressive in content and form, this text successfully bridges the gap between the circuit perspective and system perspective of digital integrated circuit design. Beginning

with solid discussions on the operation of electronic devices and in-depth analysis of the nucleus of digital design, the text maintains a consistent, logical flow of subject matter throughout. The revision addresses today's most significant and compelling industry topics, including: the impact of interconnect, design for low power, issues in timing and clocking, design methodologies, and the tremendous effect of design automation on the digital design perspective. The revision reflects the ongoing evolution in digital integrated circuit design, especially with respect to the impact of moving into the deep-submicron realm.

Digital integrated Circuits Springer

In recent years, it was realized that the MIMO communication systems seems to be inevitable in accelerated evolution of high data rates applications due to their potential to dramatically increase the spectral efficiency and simultaneously sending individual information to the corresponding users in wireless systems. This book, intends to provide highlights of the current research topics in the field of MIMO system, to offer a snapshot of the recent advances and major issues faced today by the researchers in the MIMO related areas. The book is written by specialists working in universities and research centers all over the world to cover the fundamental principles and main advanced topics on high data rates wireless communications systems over MIMO channels. Moreover, the book has the advantage of providing a collection of applications that are completely independent and self-contained; thus, the interested reader can choose any chapter and skip to another without losing continuity.

Advanced Topics in Microelectronics and System Design Cuvillier Verlag

This book describes the design of CMOS circuits for ultra-low power consumption including analog, radio frequency (RF), and digital signal processing circuits (DSP). The book addresses issues from circuit and system design to production design, and applies the ultra-low power circuits described to systems for digital hearing aids and capsule endoscope devices. Provides a valuable introduction to ultra-low power circuit design, aimed at practicing design engineers; Describes all key building blocks of ultra-low power circuits, from a systems perspective; Applies circuits and systems described to real product examples such as hearing aids and capsule endoscopes.

Digital Integrated Circuits Springer Science & Business Media

Beginning with discussions on the operation of electronic devices and analysis of the nucleus of digital design, the text addresses: the impact of interconnect, design for low power, issues in timing and clocking, design methodologies, and the effect of design automation on the digital design perspective.

Computer Vision and Information Technology Springer

China, India, and East and Southeast Asia: Assessing Sustainability provides unprecedented analyses by regional experts and scholars elsewhere in the world on China, India, and their neighbors. Despite growing demands internally on their natural resources (China and India alone are home to more than one-third of the world's population), the expanding global economic influence of this region makes these countries vital players in a sustainable future for all citizens of the Earth. Regional coverage includes topics such as business and commerce, environmental and corporate law, and lifestyles and values.

60-GHz CMOS Phase-Locked Loops Walter de Gruyter GmbH & Co KG
RFID transponders that are based on polymer integrated circuits have the potential to be produce d at high volume and low cost, due to the usage of soluble polymer semiconducting materials in printing processes. In this work, the concept of designing and simulating a passive polymer RFID transponder is presented. Models of the component soft he overall RFID-system, consisting of the reader and the polymer transponder, are derived. Simulation and measurement match well and show that inductive coupled polymer transponders can be operated at the standardized frequency of 13.56 MHz with a read range of at east 5cm. The read range is basically limited by the antenna design and the polymer rectifier. With the realized system simulation, the information transmission from the transponder to the reader can be simulated for various antenna designs, coding schemes and perturbations due to motion of the transponder.
Cryptographic Hardware and Embedded Systems - CHES 2005 Springer Science & Business Media
This book contains all the topics of importance to the low power designer. It first lays the foundation and then goes on to detail the design process. The book also discusses such special topics as power management and modal design, ultra low power, and low power design methodology and flows. In addition, coverage includes projections of the future and case studies.
Design and Analysis of High Efficiency Line Drivers for xDSL Springer
WelcometotheproceedingsofPATMOS2004,thefourteenthinaseries ofint- national workshops. PATMOS 2004 was organized by the University of Patras with technical co-sponsorship from the IEEE Circuits and Systems Society. Over the years, the PATMOS meeting has evolved into an important - ropean event, where industry and academia meet to discuss power and timing aspects in modern integrated circuit and system design. PATMOS provides a forum for researchers to discuss and investigate the emerging challenges in - sign methodologies and tools required to develop the upcoming generations of integrated circuits and systems. We realized this vision this year by providing a technical program that contained state-of-the-art technical contributions, a keynote speech, three invited talks and two embedded tutorials. The technical program focused on timing, performance and power consumption, as well as architectural aspects, with particular emphasis on modelling, design, charac- rization, analysis and optimization in the nanometer era. This year a record 152 contributions were received to be considered for p- sible presentation at PATMOS. Despite the choice for an intense three-day m- ting, only 51 lecture papers and 34 poster papers could be accommodated in the single-track technical program. The Technical Program Committee, with the - sistance of additional expert reviewers, selected the 85 papers to be presented at PATMOS and organized them into 13 technical sessions. As was the case with the PATMOS workshops, the review process was anonymous, full papers were required, and several reviews were received per manuscript.
2011 International Conference in Electrics, Communication and Automatic Control Proceedings Cambridge University Press
This book presents hardware-efficient algorithms and FPGA implementations for two robotic tasks, namely exploration and

landmark determination. The work identifies scenarios for mobile robotics where parallel processing and selective shutdown offered by FPGAs are invaluable. The book proceeds to systematically develop memory-driven VLSI architectures for both the tasks. The architectures are ported to a low-cost FPGA with a fairly small number of system gates.

Multi-Core Embedded Systems Digital Integrated Circuits Digital Integrated CircuitsPrentice Hall

Robotic Exploration and Landmark Determination Springer Science & Business Media

The 3rd Annual International Conference on Design, Manufacturing and Mechatronics (ICDMM2016) was successfully held in Wuhan, China in 2016. The ICDMM2016 covers a wide range of fundamental studies, technical innovations and industrial applications in industry design, manufacturing and mechatronics. The ICDMM2016 program consists of 4 keynote speeches, 96 oral and poster presentations. We were pleased to have more than 80 participants from China, South Korea, Taiwan, Japan, Malaysia, and Saudi Arabia. However, finally, only 83 articles were selected after peer review to be included in this proceedings.