Systematic Design Of Analog Ip Blocks

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Electronic Design
Systematic Design of Sigma-Delta Analog-to-Digital Converters
Low-Power Low-Voltage Sigma-Delta Modulators in Nanometer CMOS
EDN, Electrical Design News
EDA for IC Implementation, Circuit Design, and Process Technology
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High-Speed Photodiodes in Standard CMOS Technology
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Low-Power Deep Sub-Micron CMOS Logic
Design of Wireless Autonomous Datalogger IC's
Systematic Modeling and Analysis of Telecom Frontends and their Building Blocks
The 5th IEE International Conference on ADDA 2005
Low-Voltage CMOS Log Companding Analog Design
Low Power Analog CMOS for Cardiac Pacemakers
CMOS Analog Circuit Design
Static and Dynamic Performance Limitations for High Speed D/A Converters
VLSI Circuits and Systems
Mixed-Signal Layout Generation Concepts
The British National Bibliography
Analog Integrated Circuit Design by Simulation: Techniques, Tools, and Methods
Dynamic Characterisation of Analogue-to-Digital Converters
System Level Mixed Signal Design with Analog Platforms
Proceedings
Systematic Design of Analog IP Blocks
Systematic Design of Analog CMOS Circuits
LNA-ESD Co-Design for Fully Integrated CMOS Wireless Receivers

PEARSON BRENDAN

Matching Properties of Deep Sub-Micron MOS Transistors Springer Science & Business Media
This book introduces a design methodology that can help to bridge the productivity gap. Two different types of designs, depending on the design challenge, have been identified. To validate the presented methodologies, the authors have selected and designed accordingly three different industrial-strength applications.
Electronic Design Springer Science & Business Media
ADDA is a forum where experts in the field meet and exchange information on the developments in this field. Due to recent growth in advanced Analogue to Digital and Digital to Analogue, the topics covered were conversion techniques, applications, calibration, testing standardisation and performance. There is continuous improvement of higher speed and longer scale length devices together with new processing techniques to put more and more performance on 'the chip'. Together with this, new techniques are being developed into new applications. The driving force is the relentless move to replace analogue circuitry with digital.
Systematic Design of Sigma-Delta Analog-to-Digital Converters Springer Science & Business Media
Operational Amplifier Speed and Accuracy Improvement proposes a new methodology for the design of analog integrated circuits. The usefulness of this methodology is demonstrated through the design of an operational amplifier. This methodology consists of the following iterative steps: description of the circuit functionality at a high level of abstraction using signal flow graphs; equivalent transformations and modifications of the graph to the form where all important parameters are controlled by dedicated feedback loops; and implementation of the structure using a library of elementary cells. Operational Amplifier Speed and Accuracy Improvement shows how to choose structures and design circuits which improve an operational amplifier's important parameters such as speed to power ratio, open loop gain, common-mode voltage rejection ratio, and power supply rejection ratio. The same approach is used to design clamps and limiting circuits which improve the performance of the amplifier outside of its linear operating region, such as slew rate enhancement, output short circuit current limitation, and input overload recovery.
Low-Power Low-Voltage Sigma-Delta Modulators in Nanometer CMOS Springer Science & Business Media
This practical guide and introduction to the design of key RF building blocks used in high data rate transmitters emphasizes CMOS circuit techniques applicable to oscillators and upconvertors. The book is written in an easily accessible manner, without losing detail on the technical side.
EDN, Electrical Design News Springer Science & Business Media
Design of Wireless Autonomous Dataloggers IC's reveals the state of the art in the design of complex dataloggers, with a special focus on low power consumption. The emphasis is on autonomous dataloggers for stand-alone applications with remote reprogrammability. The book starts with a comprehensive introduction on the most important design aspects and trade-offs for miniaturized low-power telemetric dataloggers. After the general introduction follows an in-depth case study of an autonomous CMOS datalogger IC for the registration of in vivo loads on oral implants. After tackling the design of the datalogger on the system level, the design of the different building blocks is elaborated in detail, with emphasis on low power. A clear overview of the operation, the implementation, and the most important design considerations of the building blocks to achieve optimal system performance is given. Design of Wireless Autonomous Dataloggers IC's discusses the design of correlated double sampling amplifiers and sample-and-holds, binary-weighted current steering DACs, successive approximation ADCs and relaxation clock oscillators and can also be used as a manual for the design of these building blocks. Design of Wireless Autonomous Dataloggers IC's covers the complete design flow of low-power miniaturized autonomous dataloggers with a bi-directional wireless link and on-board data processing, while providing detailed insight into the most critical design issues of the different building blocks. It will allow you to design complex dataloggers faster. It is essential reading for analog design engineers and researchers in the field of miniaturized dataloggers and is also suitable as a text for an advanced course on the subject.
EDA for IC Implementation, Circuit Design, and Process Technology Springer Science & Business Media
This hands-on guide contains a fresh approach to efficient and insight-driven integrated circuit design in nanoscale-CMOS. With downloadable MATLAB code and over forty detailed worked examples, this is essential reading for professional engineers, researchers, and graduate students in analog circuit design.
Systematic Design of SIGMA-Delta Analog-To-Digital Converters Springer Science & Business Media
Presenting a comprehensive overview of the design automation algorithms, tools, and methodologies used to design integrated circuits, the Electronic Design Automation for Integrated Circuits Handbook is available in two volumes. The second volume, EDA for IC Implementation, Circuit Design, and Process Technology, thoroughly examines real-time logic to GDSII (a file format used to transfer data of semiconductor physical layout), analog/mixed signal design, physical verification, and technology CAD (TCAD). Chapters contributed by leading experts authoritatively discuss design for manufacturability at the nanoscale, power supply network design and analysis, design modeling, and much more. Save on the complete set.
Design of Very High-Frequency Multirate Switched-Capacitor Circuits Springer Science & Business Media
Systematic Design of Analog CMOS CircuitsCambridge University Press
High-Speed Photodiodes in Standard CMOS Technology Springer Science & Business Media
To meet the demands of today's highly competitive market, analog electronics designers must develop their IC designs in a minimum of time. The difference between first- and second-time right seriously affects a company's share of the market. Analog designers are therefore in need for structured design methods together with the theory and tools to support them, especially when pushing the performance limits in high-performance designs. Systematic Modeling and Analysis of Telecom Frontends and Their Building Blocks aims to help designers in speeding up

telecommunication frontend design by offering an in-depth understanding of the frontend's behavior together with methods and algorithms that support designers in bringing this understanding to practice. The book treats topics such as time-varying phase-locked loop stability, noise in mixing circuits, oscillator injection locking, oscillator phase noise behavior, harmonic oscillator dynamics and many more. In doing so, it always starts from a theoretical foundation that is both rigorous and general. Phase-locked loop and mixer analysis, for example, are grounded upon a general framework for time-varying small-signal analysis. Likewise, analysis of harmonic oscillator transient behavior and oscillator phase noise analysis are treated as particular applications of a general framework for oscillator perturbation analysis. In order to make the book as easy to read as possible, all theory is always accompanied by numerous examples and easy-to-catch intuitive explanations. As such, the book is suited for both computer-aided design engineers looking for general theories and methods, either as background material or for practical implementation in tools, as well as for practicing circuit designers looking for help and insight in dealing with a particular application or a particular high-performance design problem.
Springer Science & Business Media
This volume emphasizes the design and development of advanced switched-opamp architectures and techniques for low-voltage low-power switched-capacitor systems. It presents a novel multi-phase switched-opamp technique together with new system architectures that are critical in improving significantly the performance of switched-capacitor systems at low supply voltages.
SBCCI 2000 Springer Science & Business Media
Design of Very High-Frequency Multirate Switched-Capacitor Circuits presents the theory and the corresponding CMOS implementation of the novel multirate sampled-data analog interpolation technique which has its great potential on very high-frequency analog frond-end filtering due to its inherent dual advantage of reducing the speed of data-converters and DSP core together with the specification relaxation of the post continuous-time filtering. This technique completely eliminates the traditional phenomenon of sampled-and-hold frequency-shaping at the lower input sampling rate. Also, in order to tackle physical IC imperfections at very high frequency, the state-of-the-art circuit design and layout techniques for high-speed Switched-Capacitor (SC) circuits are comprehensively discussed: -Optimum circuit architecture tradeoff analysis -Simple speed and power trade-off analysis of active elements -High-order filtering response accuracy with respect to capacitor-ratio mismatches -Time-interleaved effect with respect to gain and offset mismatch -Time-interleaved effect with respect to timing-skew and random jitter with non-uniformly holding -Stage noise analysis and allocation scheme -Substrate and supply noise reduction -Gain-and offset-compensation techniques -High-bandwidth low-power amplifier design and layout -Very low timing-skew multiphase generation Two tailor-made optimum design examples in CMOS are presented. The first one achieves a 3-stage 8-fold SC interpolating filter with 5.5MHz bandwidth and 108MHz output sampling rate for a NTSC/PAL CCIR 601 digital video at 3 V. Another is a 15-tap 57MHz SC FIR bandpass interpolating filter with 4-fold sampling rate increase to 320MHz and the first-time embedded frequency band up-translation for DDFS system at 2.5V. The corresponding chip prototype achieves so far the highest operating frequency, highest filter order and highest center frequency with highest dynamic range under the lowest supply voltage when compared to the previously reported high-frequency SC filters in CMOS.
IEICE Transactions on Electronics CRC Press
In this book, innovative research using artificial neural networks (ANNs) is conducted to automate the placement task in analog integrated circuit layout design, by creating a generalized model that can generate valid layouts at push-button speed. Further, it exploits ANNs' generalization and push-button speed prediction (once fully trained) capabilities, and details the optimal description of the input/output data relation. The description developed here is chiefly reflected in two of the system's characteristics: the shape of the input data and the minimized loss function. In order to address the latter, abstract and segmented descriptions of both the input data and the objective behavior are developed, which allow the model to identify, in newer scenarios, sub-blocks which can be found in the input data. This approach yields device-level descriptions of the input topology that, for each device, focus on describing its relation to every other device in the topology. By means of these descriptions, an unfamiliar overall topology can be broken down into devices that are subject to the same constraints as a device in one of the training topologies. In the experimental results chapter, the trained ANNs are used to produce a variety of valid placement solutions even beyond the scope of the training/validation sets, demonstrating the model's effectiveness in terms of identifying common components between newer topologies and reutilizing the acquired knowledge. Lastly, the methodology used can readily adapt to the given problem's context (high label production cost), resulting in an efficient, inexpensive and fast model.
CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters McGraw Hill Professional
These papers are taken from 13th Brazilian Symposium on Integrated Circuit Design (SBCCI 2000). They address issues such as: microarchitectures-architecture; logic design; analogue design; high-level synthesis; digital design; physical modelling; reconfigurable hardware; and more.
Wideband Low Noise Amplifiers Exploiting Thermal Noise Cancellation CRC Press
This book presents a framework for the reuse-based design of AMS circuits. The framework is founded on three key elements: (1) a CAD-supported hierarchical design flow; (2) a complete, clear definition of the AMS reusable block; (3) the design for a reusability set of tools, methods, and guidelines. The book features a detailed tutorial and in-depth coverage of all issues and must-have properties of reusable AMS blocks.
High Data Rate Transmitter Circuits Taylor & Francis US
CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters describes in depth converter specifications like Effective Number of Bits (ENOB), Spurious Free Dynamic Range (SFDR), Integral Non-Linearity (INL), Differential Non-Linearity (DNL) and sampling clock jitter requirements. Relations between these specifications and practical issues like matching of components and offset parameters of differential pairs are derived. CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters describes the requirements of input and signal reconstruction filtering in case a converter is applied into a signal processing system. CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters describes design details of high-speed A/D and D/A converters, high-resolution A/D and D/A converters, sample-and-hold amplifiers, voltage and current references,

noise-shaping converters and sigma-delta converters, technology parameters and matching performance, comparators and limitations of comparators and finally testing of converters.
BMAS ... Springer Science & Business Media
Low Noise Amplifiers (LNAs) are commonly used to amplify signals that are too weak for direct processing for example in radio or cable receivers. Traditionally, low noise amplifiers are implemented via tuned amplifiers, exploiting inductors and capacitors in resonating LC-circuits. This can render very low noise but only in a relatively narrow frequency band close to resonance. There is a clear trend to use more bandwidth for communication, both via cables (e.g. cable TV, internet) and wireless links (e.g. satellite links and Ultra Wideband Band). Hence wideband low-noise amplifier techniques are very much needed. Wideband Low Noise Amplifiers Exploiting Thermal Noise Cancellation explores techniques to realize wideband amplifiers, capable of impedance matching and still achieving a low noise figure well below 3dB. This can be achieved with a new noise cancelling technique as described in this book. By using this technique, the thermal noise of the input transistor of the LNA can be cancelled while the wanted signal is amplified! The book gives a detailed analysis of this technique and presents several new amplifier circuits. This book is directly relevant for IC designers and researchers working on integrated transceivers. Although the focus is on CMOS circuits, the techniques can just as well be applied to other IC technologies, e.g. bipolar and GaAs, and even in discrete component technologies.
Operational Amplifier Speed and Accuracy Improvement Springer Science & Business Media
this book is not suitable for the bookstore catalogue
Analog IC Placement Generation via Neural Networks from Unlabeled Data Springer Science & Business Media
Publisher's Note: Products purchased from Third Party sellers are not guaranteed by the publisher for quality, authenticity, or access to any online entitlements included with the product. Learn the principles and practices of simulation-based analog IC design This comprehensive textbook and on-the-job reference offers clear instruction on analog integrated circuit design using the latest simulation techniques. Ideal for graduate students and professionals alike, the book shows, step by step, how to develop and deploy integrated circuits for cutting-edge Internet of Things (IoT) and other applications. Analog Integrated Circuit Design by Simulation: Techniques, Tools, and Methods lays out practical, ready-to-apply engineering strategies. Application layer, device layer, and circuit layer IC design are covered in complete detail. You will learn how to tackle real-world design problems and avoid long cycles of trial and error. Coverage includes: •First-order DC response•Unified closed-loop model•Accurate modeling of DC response•Frequency and step response•Multi-pole dynamic response and stability•Effect of external network on differential gain•Continuous-time and discrete-time amplifiers•MOSFET, NMOS, and PMOS characteristics•Small-signal modeling and circuit analysis•Resistor and capacitor design•Current sources, sinks, and mirrors•Basic, symmetrical, folded-cascode, and Miller OTAs•Opamps with source-follower and common-source output stages•Fully differential OTAs and opamps
Reuse-Based Methodologies and Tools in the Design of Analog and Mixed-Signal Integrated Circuits Springer Science & Business Media
Low Power Analog CMOS for Cardiac Pacemakers proposes new techniques for the reduction of power consumption in analog integrated circuits. Our main example is the pacemaker sense channel, which is representative of a broader class of biomedical circuits aimed at qualitatively detecting biological signals. The first and second chapters are a tutorial presentation on implantable medical devices and pacemakers from the circuit designer point of view. This is illustrated by the requirements and solutions applied in our implementation of an industrial IC for pacemakers. There from, the book discusses the means for reduction of power consumption at three levels: base technology, power-oriented analytical synthesis procedures and circuit architecture.
Analog/RF and Mixed-Signal Circuit Systematic Design Springer Science & Business Media
Matching Properties of Deep Sub-Micron MOS Transistors examines this interesting phenomenon. Microscopic fluctuations cause stochastic parameter fluctuations that affect the accuracy of the MOSFET. For analog circuits this determines the trade-off between speed, power, accuracy and yield. Furthermore, due to the down-scaling of device dimensions, transistor mismatch has an increasing impact on digital circuits. The matching properties of MOSFETs are studied at several levels of abstraction: A simple and physics-based model is presented that accurately describes the mismatch in the drain current. The model is illustrated by dimensioning the unit current cell of a current-steering D/A converter. The most commonly used methods to extract the matching properties of a technology are bench-marked with respect to model accuracy, measurement accuracy and speed, and physical contents of the extracted parameters. The physical origins of microscopic fluctuations and how they affect MOSFET operation are investigated. This leads to a refinement of the generally applied 1/area law. In addition, the analysis of simple transistor models highlights the physical mechanisms that dominate the fluctuations in the drain current and transconductance. The impact of process parameters on the matching properties is discussed. The impact of gate line-edge roughness is investigated, which is considered to be one of the roadblocks to the further down-scaling of the MOS transistor. Matching Properties of Deep Sub-Micron MOS Transistors is aimed at device physicists, characterization engineers, technology designers, circuit designers, or anybody else interested in the stochastic properties of the MOSFET.